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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application Number	10/040,596
Filing Date	December 28, 2001
First Named Inventor	Lyn Mark Elzinga
Art Unit	2825
Examiner Name	Vuthe Siek
Attorney Docket Number	42390.P13294

Total Number of Pages in This Submission: 96

ENCLOSURES *(Check all that apply)*

- [✓] Fee Transmittal Form
- [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
- [ ] After Allowance communication to Technology Center (TC)
- [ ] Appeal Communication to Board of Appeals and Interferences
- [✓] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Other Enclosure(s) (please identify below):

Remarks

Appeal Brief in support of Appeal from Final Office Action mailed 1/28/04.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	BLAKELY SOKOLOFF TAYLOR & ZAFMAN Lawrence M. Mennemeier Reg. No. 51,003
Signature	
Date	6-25-2004

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PTO/SB/17 (10-03)
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FEE TRANSMITTAL for FY 2004

Effective 10/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 300

Complete if Known	
Application Number	10/040,536
Filing Date	December 28, 2001
First Named Inventor	Lyn Mark Elzinga
Examiner Name	Vuthe Siek
Art Unit	2825
Attorney Docket No.	42390.P13294

METHOD OF PAYMENT *(check all that apply)*

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FEE CALCULATION

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1002	340	2002	170	Design filing fee	
1003	530	2003	265	Plant filing fee	
1004	770	2004	385	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X	=
Independent Claims		-3** =		X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	86	2201	43	Independent claims in excess of 3
1203	290	2203	145	Multiple dependent claim, if not paid
1204	86	2204	43	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

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FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	420	2252	210	Extension for reply within second month	
1253	950	2253	475	Extension for reply within third month	
1254	1,480	2254	740	Extension for reply within fourth month	
1255	2,010	2255	1,005	Extension for reply within fifth month	
1401	330	2401	165	Notice of Appeal	
1402	330	2402	165	Filing a brief in support of an appeal	300
1403	290	2403	145	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,330	2453	665	Petition to revive - unintentional	
1501	1,330	2501	665	Utility issue fee (or reissue)	
1502	480	2502	240	Design issue fee	
1503	640	2503	320	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	770	2809	385	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	770	2810	385	For each additional invention to be examined (37 CFR 1.129(b))	
1801	770	2801	385	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

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(Complete if applicable)

SUBMITTED BY					
Name (Print/Type)	Lawrence M. Mennemeier	Registration No. (Attorney/Agent)	51,003	Telephone	408 765-2194
Signature				Date	6-25-2004

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PTO/SB/17 (10-03)
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Examiner Name	Vuthe Siek
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Attorney Docket No.	42390.P13294

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FEE CALCULATION (continued)

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Other fee (specify)

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 300

(Complete *if applicable*)

SUBMITTED BY				
Name (Print/Type)	Lawrence M. Mennemeier	Registration No. (Attorney/Agent)	51,003	Telephone 408 765-2194
Signature				Date 6-25-2004

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Docket No.: 42390.P13294

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:
Lyn Mark Elzinga

Application No. 10/040,536

Filed: December 28, 2001

For: INTERCONNECT SWIZZLING FOR CAPACATIVE AND INDUCTIVE NOISE CANCELLATION

Examiner: Vuthe Siek

Art Unit: 2825

CERTIFICATE OF TRANSMISSION

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on 6/25/04 Lawrence M. Mennemeier
Date

APPELLANT'S BRIEF UNDER 37 CFR § 1.192 IN SUPPORT OF APPELLANT'S APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Mail Stop Appeal Brief-Patents
Commissioner of Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellant hereby submits this Brief in triplicate in support of an appeal from a final decision of the Examiner, in the above-referenced case. Appellant respectfully requests consideration of this appeal by the board of Patent Appeals and Interference for allowance of the above-referenced patent application.

TABLE OF CONTENTS

I. Real Party in Interest

The real party in interest in the present appeal is Intel Corporation of Santa Clara, California, the assignee of the present application.

II. Related Appeals and Interferences

There are no related appeals or interferences to appellant's knowledge that would have a bearing on any decision of the Board of Patent Appeals and Interferences.

III. Status of the Claims

Claims 1-23 and 26-38 are allowed

Claims 24 and 25 stand rejected under 35 USC § 102(b) as allegedly being anticipated by US Patent 5,534,732 (DeBrosse).

IV. Status of Amendments

A preliminary amendment, submitted by appellant on 6/7/2002 was entered. An official response to a first Office Action mailed 7/15/2003 was submitted by appellant on 11/17/2003 and was entered. A Final Office Action was mailed on 1/28/2004. Appellant responded by submitting an amendment and official response after final on 3/23/2004, which was entered and an Advisory Action was mailed 5/4/2004. A Notice of Appeal was transmitted on 4/28/2004, and an appeal ensued.

Accordingly, the claims stand as of the entered amendment of 3/23/2004, and are reproduced in clean form in the Appendix.

V. Summary of the Invention

Appellant's disclosure describes a process to employ swizzling that provides capacitive and inductive noise cancellation on a set of concurrently active signal lines. A positive noise due to a capacitive coupling between an attacker signal line and a near victim signal line is, in part, cancelled by a negative or opposite noise due to an inductive coupling between the attacker signal line and a far victim signal line. A swizzling pattern is set forth whereby signal lines of one segment are reordered to transpose near victim signal lines and far victim signal lines in subsequent segments to facilitate the capacitive and inductive cancellation. The swizzling pattern is selected to further facilitate similar capacitive and inductive noise cancellation among the other signal lines of the set.

In some embodiments, the process continues to employ the swizzling pattern in multiple stages to place each signal line adjacent to every other signal line of the set in some swizzle stage. In some alternative embodiments, swizzling patterns may be selected which place each signal line adjacent to every other signal line of the set in some predetermined number of swizzle stages. Subsequent stages of swizzling provide the set of signal lines with capacitive and inductive noise cancellation in addition to the capacitive and inductive noise cancellations of previous stages. The signal lines are optionally reordered by a final swizzle stage to restore the set's original order. In some embodiments, swizzling patterns may be selected from cyclic swizzle groups such that repeating the swizzling pattern automatically restores the set's original order and/or places each signal line adjacent to other signal lines of the set in a predetermined number of swizzle stages.

In some embodiments, a plurality of S swizzle stages may be inserted to provide capacitive and inductive noise cancellation within a set of N concurrently active signal lines, S being computed for a particular value of N according to the equation:

$$N^2/2 - (2S+3)N/2 + S + 1 = 0.$$

VI. Issues

1. Is claim 24 anticipated by DeBrosse?

2. Is claims 25 anticipated by DeBrosse?

VII. Grouping of Claims (Independent Claims **Bolded**)

For the purposes of this appeal, claims **24** and 25 do not stand or fall together.

Group I: Means for Providing Multiple Capacitive and Inductive Noise Cancellation Stages.

Claim **24**.

Group II: Means for Providing Multiple Capacitive and Inductive Noise Cancellation Stages and Restoring Initial Order.

Claim 25.

VIII. Argument

A. Claim 24 Is Not Anticipated by DeBrosse

Claim 24 stands rejected under 35 USC § 102(b) as allegedly being anticipated by US Patent 5,534,732 (DeBrosse).

The MPEP § 2131 states that:

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Appellant respectfully submits that in the cited reference, each and every element as set forth in the Group I claim is not found, either expressly or inherently described.

Claim 24, for example, sets forth:

24. (Original) An interconnect comprising:
a set of N active signal lines having an initial order;
means for providing the set of signal lines with a first capacitive and inductive noise cancellation; and;
means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation.

The invention of DeBrosse relates to a single crossing region that traverses paired true/complement line conductors such that intra-pair capacitive coupling is avoided and inter-pair capacitive coupling is matched (abstract; col. 2, lines 47-51; Figs 5 and 7-10).

The Final Office Action states (emphasis added):

"DeBrosse et al. teach an interconnection layout comprising a set of N active signal lines having an initial order (as shown in Figure 5 for example); means for providing the set of signal lines with a first capacitive and inductive noise cancellation; and means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation (shown in Figure 5 for example). DeBrosse et al. show capacitive noise cancellation. Since capacitive and inductive parasitics are inherently included in conductive line[s], thus capacitive noise cancellation inherently includes inductive noise cancellation."

Appellant respectfully disagrees. Appellant submits that (1) in the first region of

DeBrosse, the signal lines are in their initial order where DeBrosse states that intra-pair capacitive coupling between true and complement lines is avoided not cancelled (col. 6, lines 1-23; Fig. 5).

Appellant further submits that (2) in the second region of DeBrosse, capacitive coupling between pairs is matched such that a line which was disposed adjacent to a true signal line of a pair in the first region is then disposed adjacent to the complemented signal line of the pair in the second region and vise-versa. For example the signal labeled 2-bar is adjacent to the signals labeled 1-bar and 3 in the first region and then adjacent to their complements labeled 1 and 3-bar in the second region (Fig. 5). Thus, in DeBrosse, the set of signal lines is provided with a single cancellation of the capacitive couplings from the true and complemented signal lines (col. 6, lines 1-27; Fig. 5).

On the other hand, claim 24 sets forth means for providing the set of signal lines with a first capacitive and inductive noise cancellation, and means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation. DeBrosse does not describe, either expressly or inherently, providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation.

Appellant further submits that (3) from the presence of inductive parasitics in line conductors it can not be concluded that capacitive noise cancellation inherently includes inductive noise cancellation.

In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999):

> To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by

persons of ordinary skill." Continental Can Co. v. Monsanto Co. , 948 F.2d 1264, 1268, 20 U.S.P.Q.2d 1746, 1749 (Fed. Cir. 1991).

The existence of inductive parasitics does not make it clear that the missing descriptive matter, "capacitive and inductive noise cancellation," is necessarily present in the technique described in the reference. The examiner does not provide objective evidence or cogent technical reasoning to support the conclusion of inherency. Capacitive coupling is strongly related to the proximity of the signal lines, which is addressed by DeBrosse. On the other hand, for inductive coupling it is not so much the proximity of a signal line to an attacker signal line as it is the surface area of a current loop or current loops formed by the attacker signal line and its closest return path, which is not addressed by DeBrosse. One signal line may be inductively coupled to many or all of the other signal lines and DeBrosse addresses only adjacent signal lines and their paired complement signal lines.

Appellant provides the following article as extrinsic evidence that the missing descriptive matter would not be recognized by one of skill in the art as being necessarily present in the technique described by DeBrosse.

Exhibit A: Guoan Zhong et al., A Twisted-Bundle Layout Structure for Minimizing Inductive Coupling Noise, *International Conference on Computer-Aided Design*, Nov. 5-9, 2000.

Referring to subsection 4.2 titled "Caveats," paragraphs 2 and 3 and Figure 5, the authors address the question of whether it is possible to reduce mutual inductances within a group of signal lines sharing a common return (such as the one shown in Fig. 11 of DeBrosse) by reordering the positions of signal lines within the group. They conclude that it is not.

Finally, appellant submits that (4) DeBrosse should not be considered equivalent

under 35 U.S.C. 112, paragraph six, to the subject matter set forth in claim 24.

The MPEP § 2181 states that:

> When making a determination of patentability under 35 U.S.C 102 or 103, past practice was to interpret a "means or step plus function" limitation by giving it the "broadest reasonable interpretation." Under the PTO's long-standing practice this meant interpreting such a limitation as reading on any prior art means or step which performed the function specified in the claim without regard for whether the prior art means or step was equivalent to the corresponding structure, material or acts described in the specification. However, in Donaldson, the Federal Circuit stated:
>
> Per our holding, the "broadest reasonable interpretation" that an examiner may give means-plus-function language is that statutorily mandated in paragraph six. Accordingly, the PTO may not disregard the structure disclosed in the specification corresponding to such language when rendering a patentability determination.

While appellant intends that the broadest reasonable interpretation should be given to claims 1-23 and 28-38, all of which have been allowed, the means-plus-function form of claim 24 may not be modified by language containing sufficient structure, material or acts for achieving the specified function. Therefore claim 24 should be construed to cover the corresponding structure, material or acts described in the specification and equivalents thereof.

The MPEP § 2181 also states that:

> [U]nless an element performs the identical function specified in the claim, it cannot be an equivalent for the purposes of 35 U.S.C. 112, sixth paragraph. Pennwalt Corp. v. Durand-Wayland, Inc., 833 F.2d 931, 4 USPQ2d 1737 (Fed. Cir. 1987), cert. denied, 484 U.S. 961 (1988).

For example, as described in paragraph [0041] of the specification for the present application, in a process to employ swizzling that may provide capacitive and inductive noise cancellation on a set of signal lines, a positive noise due to a capacitive coupling between an attacker signal line and a first victim signal line is, in part, cancelled by a negative or opposite noise due to an inductive coupling between the attacker signal line and a second victim signal line.

Paragraph [0046] explains a key observation is that by reversing the positions of

the near victim signal line and far victim signal line with respect to the attacker in a subsequent interconnect segment, a partial cancellation of the capacitive and inductive noise voltages may be provided. Therefore, it will be appreciated that a partial cancellation of capacitive and inductive noise may be provided in a subsequent interconnect segment by a swizzling of a set of signal lines.

Paragraph [0049] also explains that typically the inductive noise from one attacker is weaker than the capacitive noise form one attacker. A key observation is that additional swizzling may be used to provide subsequent stages of further capacitive and inductive noise cancellation for the set by balancing the number of signal lines that are near neighbors in subsequent stages.

DeBrosse does not suggest capacitive and inductive noise cancellation as disclosed in appellant's specification or equivalents thereof, but rather shows a technique for avoidance of capacitive coupling between pairs of true/complement line conductors, and capacitive matching between the true/complement line conductors of one pair and those of its neighbor pairs (col. 1, lines 11-15, col. 2, lines 56-67 and col. 3, lines 1-5). DeBrosse admits that his layout is applicable only to interconnection arrays having a plurality of paired true/complement line conductors (col. 3, lines 28-30).

Appellant respectfully submits that a person of ordinary skill in the art would not have recognized an interchangeability of DeBrosse (which relies upon capacitive matching between the true/complement line conductor pairs) and the capacitive and inductive noise cancellation disclosed in appellant's specification (which does not rely upon such characteristics of true/complement line conductors).

Even if capacitive matching between the true/complement line conductors could

be considered equivalent to the capacitive and inductive noise cancellation function set forth in claim 24, DeBrosse performed it in a substantially different way (by alternating the capacitive coupling of true and complement line conductors and requiring twice as many signal lines as the method disclosed in appellant's specification) with a substantially different result (a single crossing region versus repeatedly swizzling to balance the number of signal lines that are near neighbors for subsequent capacitive and inductive noise cancellation).

DeBrosse does not expressly or inherently describe equivalent means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation. DeBrosse shows a technique including, "forming a single crossing region including crossing the line conductors of each pair once;" (col. 3, lines 13-15). DeBrosse discloses reordering the signal lines only once (col. 3, lines 22-24 and col. 7, lines 63 through col. 8, line 2). Even DeBrosse's title, "Single Twist Layout and Method for Paired Line Conductors of Integrated Circuits," admits the nonequivalence of the prior art element of DeBrosse for allegedly performing the function set forth in claim 24.

Accordingly in light of the argument presented above, appellant respectfully submits that indcpendent claim 24 is not anticipated by DeBrosse.

B. Claim 25 Is Not Anticipated by DeBrosse

Claim 25 stands rejected under 35 USC § 102(b) as allegedly being anticipated by US Patent 5,534,732 (DeBrosse).

In accordance with the arguments presented above with regard to the patentability of claim 24, appellant believes that claim 25 is patentable, first, for including all of the limitations of claim 24, and additionally for the reasons described below.

The MPEP § 2131 states that:

> "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Appellant respectfully submits that in the cited reference, each and every element as set forth in the Group II claim is not found, either expressly or inherently described in as complete detail as is contained in the claim.

Claim 25, for example, sets forth:

> 25. (Original) The interconnect of Claim 24 further comprising:
> means for restoring the initial order of the set of signal lines.

As stated above, the invention of DeBrosse relates to a single crossing region that traverses paired true/complement line conductors such that intra-pair capacitive coupling is avoided and inter-pair capacitive coupling is matched (abstract; col. 2, lines 47-51). Clearly, the initial order of the set of signal lines is not restored by the single crossing region of DeBrosse (see for example Figs 5 and 7-10).

The Final Office Action states:

> "DeBrosse et al. teach that signal lines in the crossing region are reordered in the third region in order to obtain initial signal lines in the first region or as original signal lines configuration in initial stage, where the signal lines are substantially parallel (Please se Figs. 5, 7, 8, 9, 10 and 11)."

Appellant respectfully disagrees. Appellant submits that (1) in the first region of

DeBrosse, the signal lines are in their initial order and that initial order is not restored by any means.

Referring to Figure 5, for example, DeBrosse states that in the first region line conductor 1 is disposed adjacent to line conductor 2 and line conductor 1-bar is disposed adjacent to line conductor 2-bar (col. 6, lines 1-6). In contrast, opposite the crossing region, line conductor 1 is disposed adjacent to line conductor 2-bar and line conductor 2 is disposed adjacent to line conductor 3-bar, which is not the same order as their initial order (col. 6, lines 7-13). DeBrosse refers to the pattern applied to initially ordered lines 1, 2, 1-bar, and 2-bar respectively as "down 1," "down 3," "up 3," and "up 1," (col. 6, lines 16-17).

Further, as stated above with regard to claim 24, the means-plus-function form of claim 25 may not be modified by language containing sufficient structure, material or acts for achieving the specified function. Therefore claim 25 should be construed to cover the corresponding structure, material or acts described in the specification and equivalents thereof.

Appellant submits that (2) DeBrosse should not be considered equivalent under 35 U.S.C. 112, paragraph six, to the subject matter set forth in claim 25.

For example, as described in paragraphs [0094] and [0095] of the specification for the present application with reference to Figure 10, it will be appreciated that repeated compositions of c and d generate swizzle groups with respect to an initial order {1,2,3,4,5,6,7,8} as follows:

$$c^1 = \{7,4,1,3,6,8,5,2\}, \quad d^1 = \{2,4,1,6,3,8,5,7\},$$

$$c^2 = \{5,3,7,1,8,2,6,4\}, \quad d^2 = \{4,6,2,8,1,7,3,5\},$$

$c^3 = \{6,1,5,7,2,4,8,3\}$, $d^3 = \{6,8,4,7,2,5,1,3\}$,

$c^4 = \{8,7,6,5,4,3,2,1\}$, $d^4 = \{8,7,6,5,4,3,2,1\}$,

$c^5 = \{2,5,8,6,3,1,4,7\}$, $d^5 = \{7,5,8,3,6,1,4,2\}$,

$c^6 = \{4,6,2,8,1,7,3,5\}$, $d^6 = \{5,3,7,1,8,2,6,4\}$,

$c^7 = \{3,8,4,2,7,5,1,6\}$, $d^7 = \{3,1,5,2,7,4,8,6\}$,

$c^8 = \{1,2,3,4,5,6,7,8\}$, $d^8 = \{1,2,3,4,5,6,7,8\}$.

It will be further appreciated that a swizzling pattern given by c^1, c^1, c^1, c^5, may be employed using swizzling 1041 repeatedly and optionally restoring the initial order of the set using swizzling 1045.

Similarly, Figures 4a-b, 10a-c, 11b, and 13a-d illustrate alternative embodiments where the initial order of a set of signal lines may be restored by swizzling patterns which may be conveniently selected from swizzle groups.

DeBrosse does not expressly or inherently describe equivalent means for restoring the initial order of the set of signal lines. The techniques of DeBrosse use a single crossing region crossing the line conductors of each pair only once and reordering the signal lines exactly once (col. 3, lines 13-24 and col. 7, lines 63 through col. 8, line 2).

Appellant respectfully submits that a person of ordinary skill in the art would not have recognized an interchangeability of the single crossing region of DeBrosse and the swizzling patterns disclosed in appellant's specification for restoring the initial order of the set of signal lines.

Additionally, appellant believes that since the single crossing region of DeBrosse performs a substantially different function (matching true/complement signal line pairs) in a substantially different way (reordering the signal lines exactly once), it is not

equivalent for allegedly performing the function of restoring the initial order of the set of signal lines set forth in claim 25.

Accordingly in light of the argument presented above, appellant respectfully submits that dependent claim 25 is not anticipated by DeBrosse.

Conclusion

Appellant submits that all claims now pending are in condition for allowance. Such action is earnestly solicited at the earliest possible date. If there is a deficiency in fees, please charge our Deposit Acct. No. 02-2666.

Respectfully submitted,

Date: 6/25/2004

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IX. Appendix A: Claims Allowed and Involved in Appeal (Clean Copy)

1. (Original) A method comprising:

swizzling a set of N concurrently active signal lines into a first order to provide a first stage of capacitive and inductive noise cancellation for a first plurality of signal lines of the set; and

swizzling the set of N concurrently active signal lines again into a second order different from the first order to provide a second stage of further capacitive and inductive noise cancellation for the first plurality of signal lines of the set.

2. (Original) The method of Claim 1 wherein a first signal line of the set is adjacent to a first subset of the set of N concurrently active signal lines in the first stage and swizzling the set of N concurrently active signal lines again places the first signal line adjacent to a second subset of the set of N concurrently active signal lines in the second stage, the first subset and the second subset being disjoint.

3. (Original) The method of Claim 2 wherein the first signal line of the set is adjacent to a third subset of the set of signal lines in an initial order of the set of N concurrently active signal lines and swizzling the set of signal lines places the first signal line adjacent to the first subset of signal lines in the first stage, the first subset and the third subset being disjoint.

4. (Original) The method of Claim 1 wherein the set of N concurrently active signal lines have a substantially common origin and a substantially common destination.

5. (Original) The method of Claim 1 wherein swizzling the set of N concurrently active signal lines comprises reordering N signal lines for concurrently carrying N bits of information in substantially parallel signal tracks on a substantially planar substrate by

routing each of a second plurality of said N signal lines from a corresponding pre-swizzling signal track directly to a corresponding post-swizzling signal track, optionally via a substantially parallel planar layer.

6. (Original) The method of Claim 5 wherein each swizzling of the set of N concurrently active signal lines is accomplished by inserting a single swizzle cell.

7. (Original) The method of Claim 1 comprising swizzling the set of N concurrently active signal lines to provide S stages of capacitive and inductive noise cancellation and optionally providing an additional stage to restore an initial order of the set, wherein each of the N concurrently active signal lines of the set is placed adjacent to every other signal line of the set in some stage of the S stages, S being computed from N according to the equation:

$$N^2/2 - (2S+3)N/2 + S + 1 = 0.$$

8. (Original) An article of manufacture comprising

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the method of Claim 7.

9. (Original) An article of manufacture comprising

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the method of Claim 6.

10. (Original) An article of manufacture comprising

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the method of Claim 3.

11. (Original) An article of manufacture comprising

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the method of Claim 1.

12. (Original) The method of Claim 1 wherein the first stage of capacitive and inductive noise cancellation and the second stage of further capacitive and inductive noise cancellation reduce capacitive and inductive noise due to switching within the set of signal lines.

13. (Original) The method of Claim 1 wherein concurrently active indicates that each of the N signal lines may be switched in a single transmission cycle.

14. (Original) An apparatus comprising:

a set of N signal lines configurable to transmit N bits of information in a transmission cycle, the signal lines being substantially parallel and having a first portion with a first signal line order;

a first swizzle stage of the set of N signal lines having a second portion with a second signal line order, wherein a first signal line of the set is adjacent to a first subset of the N signal lines in said first portion and the first signal line is adjacent to a second subset of the N signal lines in said second portion, the first subset and the second subset being disjoint; and

a second swizzle stage of the set of N signal lines having a third portion with a third signal line order, wherein the first signal line of the set is adjacent to a third subset of the N signal lines in said third portion, the first subset the second subset and the third subset being disjoint.

15. (Original) The apparatus of Claim 14 wherein the set of N signal lines have a substantially common origin and a substantially common destination.

16. (Original) The apparatus of Claim 14 comprising

said set of N signal lines in substantially parallel signal tracks on a substantially planar substrate;

each of a first plurality of the N signal lines being routed from a corresponding

signal track in the first portion, according to the first signal line order, directly to a corresponding signal track in the second portion, according to the second signal line order, optionally via one or more substantially parallel planar layers; and

each of a second plurality of the N signal lines being routed from a corresponding signal track in the second portion, according to the second signal line order, directly to a corresponding signal track in the third portion, according to the third signal line order, optionally via the one or more substantially parallel planar layers.

17. (Original) The apparatus of Claim 14 wherein the first swizzle stage of the set of N lines comprises a swizzle cell coupling the first portion with the second portion.

18. (Original) The apparatus of Claim 17 wherein the second swizzle stage of the set of N lines comprises a swizzle cell coupling the second portion with the third portion.

19. (Original) The apparatus of Claim 14 comprising

a plurality of S swizzle stages to provide capacitive and inductive noise cancellation within the set of N signal lines, wherein each of the N signal lines of the set is placed adjacent to every other signal line of the set in some swizzle stage of the S swizzle stages, S being computed for a particular value of N according to the equation, $N^2/2 - (2S+3)N/2 + S + 1 = 0$; and

an optional final stage to restore an initial order for the set of N signal lines.

20. (Original) The apparatus of Claim 14 wherein the third portion of the second swizzle stage places no signal line, of the set of N signal lines, adjacent to one of the same signal lines that they are adjacent to in the second portion of the first swizzle stage.

21. (Original) The apparatus of Claim 20 wherein the second portion of the first swizzle stage places no signal line, of the set of N signal lines, adjacent to one of the same signal lines that they are adjacent to in the first portion.

22. (Original) The apparatus of Claim 21 wherein the third portion of the second swizzle stage places no signal line, of the set of N signal lines, adjacent to one of the same signal lines that they are adjacent to in the first portion.

23. (Original) The apparatus of Claim 14 comprising

a first swizzle cell to reorder the set of N signal lines from the first signal line order into the second signal line order;

a second swizzle cell to reorder the set of N signal lines from the second signal line order into the third signal line order; and

an optional third swizzle cell to restore an initial order for the set of N signal lines.

24. (Original) An interconnect comprising:

a set of N active signal lines having an initial order;

means for providing the set of signal lines with a first capacitive and inductive noise cancellation; and;

means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation.

25. (Original) The interconnect of Claim 24 further comprising:

means for restoring the initial order of the set of signal lines.

26. (Previously Amended) An interconnect comprising:

a set of N active signal lines having an initial order;

means for providing the set of signal lines with a first capacitive and inductive noise cancellation;

means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation; and

means for restoring the initial order of the set of signal lines, wherein the means for restoring the initial order of the set of signal lines provides the set of signal lines with a third capacitive and inductive noise cancellation in addition to the first and second

capacitive and inductive noise cancellations.

27. (Original) The interconnect of Claim 26 wherein the set of signal lines contains an even number of signal lines.

28. (Original) An article of manufacture comprising:

a machine-accessible medium including data that, when accessed by a machine, cause the machine to:

insert a first swizzle stage to provide a set of N concurrently active signal lines having a first signal line order, with a second signal line order, where in the first signal line order, a first signal line of the set is adjacent to a first subset of the N signal lines and in the second signal line order the first signal line is adjacent to a second subset of the N signal lines, the first subset and the second subset having no signal lines in common; and

insert a second swizzle stage to provide the set of N concurrently switched signal lines with a third signal line order, where in the third signal line order the first signal line is adjacent to a third subset of the N signal lines, the first subset, the second subset and the third subset having no signal lines in common.

29. (Original) The article of manufacture of Claim 28 wherein the second signal line order of the first swizzle stage provides a capacitive and inductive noise cancellation by placing the first signal line adjacent to the second subset of the N signal lines.

30. (Original) The article of manufacture of Claim 29 wherein the third signal line order of the second swizzle stage provides an additional capacitive and inductive noise cancellation by placing the first signal line adjacent to the third subset of the N signal lines.

31. (Original) The article of manufacture of Claim 30 wherein the first capacitive and inductive noise cancellation and the additional capacitive and inductive noise cancellation reduce capacitive and inductive noise due to switching within the set of N concurrently

active signal lines.

32. (Original) The article of manufacture of Claim 28 wherein the third signal line order of the second swizzle stage places no signal line, of the set of N concurrently active signal lines, adjacent to one of the same signal lines that they are adjacent to in the second signal line order of the first swizzle stage.

33. (Original) The article of manufacture of Claim 32 wherein second signal line order of the first swizzle stage places no signal line, of the set of N concurrently active signal lines, adjacent to one of the same signal lines that they are adjacent to in the first signal line order.

34. (Original) The article of manufacture of Claim 33 further including data that when accessed by the machine, cause the machine to:

insert a third swizzle stage to restore the set of N concurrently active signal lines to their original order.

35. (Original) The article of manufacture of Claim 28 wherein concurrently active indicates that each of the N signal lines may be switched in a transmission cycle.

36. (Original) The article of manufacture of Claim 28 further including data that when accessed by the machine, cause the machine to:

insert a plurality of S swizzle stages to provide capacitive and inductive noise cancellation within the set of N concurrently active signal lines, wherein each of the N signal lines of the set is placed adjacent to every other signal line of the set in some swizzle stage of the S swizzle stages, S being computed for a particular value of N according to the equation

$$N^2/2 - (2S+3)N/2 + S + 1 = 0; \text{ and}$$

insert an optional swizzle to restore an initial order for the set of N concurrently active signal lines.

37. (Original) An apparatus comprising:

a set of N concurrently active signal lines, the signal lines being substantially parallel and having a first signal line order;

a plurality of swizzle cells linking segments of the set of N concurrently active signal lines, the plurality of swizzle cells transposing near victim signal lines and far victim signal lines in subsequent segments to facilitate capacitive and inductive noise cancellation within the set of N concurrently active signal lines; and

an optional swizzle cell to restore an initial order for the set of N concurrently active signal lines.

38. (Original) The apparatus of Claim 37 wherein concurrently active indicates that each of the N signal lines may be switched in a single transmission cycle.

Exhibit A

Guoan Zhong et al., A Twisted-Bundle Layout Structure for Minimizing Inductive Coupling Noise, *International Conference on Computer-Aided Design*, Nov. 5-9, 2000.

A Twisted-Bundle Layout Structure for Minimizing Inductive Coupling Noise*

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ABSTRACT

In this paper, we propose a novel *twisted-bundle* layout structure for minimizing inductive coupling noise. In this structure, we create several routing regions and re-order the routing of nets in each of these routing regions. The purpose is to create complementary and opposite current loops in the twisted-bundle layout structure, such that the magnetic fluxes arising from any signal net within a *twisted group* cancel each other in the current loop of a net of interest. The effectiveness of the twisted-bundle structure in minimizing coupling inductance has been verified by the application of FastHenry extraction on a 16-bit bus structure. We achieve about two orders of magnitude reduction in inductive coupling. SPICE simulations also show that the 16-bit twisted-bundle bus structure is able to maintain high signal integrity at high frequency of operation.

1. INTRODUCTION

Continued scaling of semiconductor technology has brought the issues of interconnect-limited designs to the forefront. The International Technology Roadmap for Semiconductor (ITRS) [1] forecasts that as the VLSI technology advances towards giga-Hertz on-chip frequency and system-level integration on larger die size, self- and coupling-inductances are becoming dominant factors in determining signal delay and signal integrity.

Ref. [16] gave an extensive survey of various noise sources in circuit design. Predominantly, existing studies focused on cross-talk noise due to capacitive coupling. Due to the short range effect of capacitive coupling, techniques such as shielding, net ordering or track permutation have proved to be effective in minimizing capacitive cross-talk noise [6; 17].

On the other hand, inductive effects have a long range effect because they arise from the electromagnetic phenomenon of magnetic flux linking current loops. As a result, inductive noise has a much wider spatial effect than that of a capacitive noise. For this reason, it makes the worst case situation in a circuit much harder to predict. Many of the existing studies that dealt with on-chip inductive effects focused primarily on the modeling and extraction of on-chip interconnect inductance. In [15], loop inductance was calculated in terms of partial inductances defined for wire segments. The Partial Element Equivalent Circuit (PEEC) model was widely used to analyze on-chip inductance [7; 14; 4]. In [9], frequency dependent inductance and resistance were computed based on the magnetoquasistatic assumption, and in [10], a simple layout rule-based method was used to speed up the computation.

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A few recent studies have reported success in minimizing the undesirable inductive effects. In recent Alpha chip designs [2], on-chip inductance was limited by sandwiching lines with high current density between isolating metal planes. In [11], the wiring overhead was reduced by using a interdigitated layout structure, in which a wide wire was split into many lines, interspersed with ground lines. These techniques, however, considered only self-inductance. In [8], inductive coupling noise was reduced by shield insertion and net ordering.

In this paper, we propose a novel *twisted-bundle* layout structure for minimizing inductive coupling noise. By creating complementary and opposite current loops in the layout structure, we achieve two orders of magnitude reduction in inductive coupling. The abilities of the twisted-bundle structure in minimizing coupling inductance and maintaining high signal integrity have been verified by the applications of FastHenry extraction and SPICE simulations on a 16-bit bus structure.

The rest of the paper is organized as follows. In Section 2, preliminaries regarding inductive coupling are explained. In Section 3, we introduce a twisted-pair layout structure, upon which the twisted-bundle structure is based. In Section 4, we present the novel twisted-bundle structure and a systematic approach for synthesizing such a structure. In Section 5, we apply this structure to a 16-bit bus design and compare it with the "traditional" design based on the parasitic parameters extracted by FastHenry and the simulation results by SPICE. Finally, we conclude in Section 6.

2. PRELIMINARIES

Mutual inductances, as well as self inductance, are electromagnetic phenomena that arises from current loops [12; 13]. The inductances for a system of N loops are defined as:

$$L_{ij} = \frac{\psi_{ij}}{I_j}, \tag{1}$$

where ψ_{ij} is the magnetic flux in loop i due to a current I_j in loop j. L_{ii} represents the self inductance of loop i, whereas $L_{ij} (i \neq j)$ represents the mutual inductance between loops i and j.

According to the Faraday's law, the mutual inductance can be calculated by finding the magnetic flux linking one loop related to per unit of current in the other loop:

$$M = L_{ij} = \int\int_{S_i} \vec{B} \cdot d\vec{S}_i \,/\, I_j, \tag{2}$$

where B is the density of the magnetic flux arising from current I_j in loop i and the integration is over the surface of loop i.

On-chip signal nets form loops with their current return paths; these loops determine the inductances as shown in Eqns. (1) and (2). Therefore, in order to accurately calculate the inductances of

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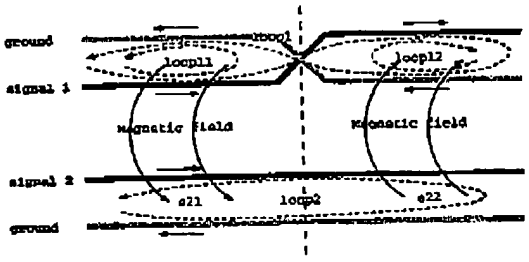

Figure 1: Twisted-pair structure.

on-chip interconnections, it is of critical importance to determine the current return paths of on-chip signal nets. However, it is extremely difficult to find accurate return paths for signal nets, because in the complex interconnection structures that we deal with today, there are several paths through which a current returns [3].

In this work, we assume that all signals use the nearest power/ground line as their return paths [5]. Although quiet or opposite-switching neighboring nets may also serve as return paths, they are not ideal because currents returning from signal wires have to go through devices, which typically have a resistance of several hundred Ohms.

3. TWISTED-PAIR LAYOUT STRUCTURE

From the Faraday's law, there are two possible ways of eliminating the coupling inductance: (i) by creating a magnetic flux that is of an opposite direction; (ii) by eliminating or minimizing the surface area of the second loop. To achieve that, we propose a simple *twisted-pair* layout structure (Figure 1) that is inspired by the twisted-pair wire structure.

As shown in Figure 1, we consider two signal lines in this structure. For each signal line, we assume that there exists a ground line nearby, serving as the signal's dedicated return path. The signal and ground lines are drawn with different shades of gray. Like the twisted-pair wire structure, we intertwine one signal line and its return path at their mid-points such that they are "symmetric" about the mid-points. As the signal and ground lines co-exist on the same metal layer, the physical layout of such a twisted-pair structure involves vias and doglegs.

As indicated in Figure 1, signal lines 1 and 2 form respectively loops $loop_1$ and $loop_2$ with their dedicated return paths. As signal 1 and its return path are twisted, $loop_1$ is divided into two smaller loops: $loop_{11}$ and $loop_{12}$. In quasi-static condition, the current is continuous everywhere along a signal line. Therefore, the two current loops flow in opposite directions, and the magnetic fields caused by $loop_{11}$ and $loop_{12}$ are equal in magnitude, but in opposite directions. According to the Faraday's law in Eqn. (2), the mutual inductance $M = L_{21}$ can be calculated by finding the magnetic flux linking $loop_1$ to $loop_2$:

$$M = \int\int_{s_2} \vec{B} \cdot d\vec{S}_2 \; / \; I_1. \qquad (3)$$

As the integration is over the surface of $loop_2$, we divide the surface of loop into two equal parts S_{21} and S_{22} along the mid-line drawn in Figure 1. We rewrite Eqn. (3) as:

$$M = (\int\int_{s_{21}} \vec{B} \cdot d\vec{S}_{21} + \int\int_{s_{22}} \vec{B} \cdot d\vec{S}_{22}) \; / \; I_1. \qquad (4)$$

When the lengths of the wires are much larger than the spacing between the wires, the magnetic flux linkage in S_{21} mainly comes from $loop_{11}$, and the magnetic flux linkage in S_{22} is primarily due to $loop_{12}$. As the current directions in $loop_{11}$ and $loop_{12}$ are opposite, the directions of the magnetic fluxes in S_{21} and S_{22} are opposite. Therefore, the two integrations over S_{21} and S_{22} cancel each other:

$$\int\int_{s_{22}} \vec{B} \cdot d\vec{S}_{22} = - \int\int_{s_{21}} \vec{B} \cdot d\vec{S}_{21}; \qquad (5)$$

Hence, the mutual inductance between signals 1 and 2 is zero:

$$M = (\int\int_{s_{21}} \vec{B} \cdot d\vec{S}_{21} - \int\int_{s_{21}} \vec{B} \cdot d\vec{S}_{21}) \; / \; I_1 = 0. \qquad (6)$$

In fact, $loop_{12}$ also contributes to the magnetic flux linkage in S_{21}. So does $loop_{11}$ to S_{22}. However, their contributions are quite insignificant, as these two components of magnetic flux also cancel each other in the integration. We can similarly argue that L_{12} is zero because the surfaces of the two loops $loop_{11}$ and $loop_{12}$ actually "sum" to zero.

All the preceding discussions are based on the assumption that the current in a signal line is continuous everywhere. However, this assumption is not valid when the wire length is sufficiently long for the transmission line effect to kick in. If parallel termination is adopted at the receiving ends of signal lines, there are no or minimal reflections at the receiving ends. Consequently, noises gathered at the victim nets cancel each other when they reach the receiving ends. Hence, the mutual inductance is still zero.

We use FastHenry [9] to verify the effectiveness of the proposed twisted-pair layout structure in minimizing coupling inductance. The wire width, height, length, and spacing are $1\mu m$, $2\mu m$, $200\mu m$, and $1\mu m$, respectively.

We extract the inductance matrix under two frequencies: a *high* frequency of $f_H = 10^{16}Hz$ and a *low* frequency of $f_L = 10^6Hz$. The inductance matrices for a *normal* or *un-twisted* structure are given below:

$f_H = 10^{16}Hz$

$$\begin{pmatrix} 7.4e-11 & 6.2e-12 \\ 6.2e-12 & 7.4e-11 \end{pmatrix}$$

$f_L = 10^6Hz$

$$\begin{pmatrix} 9.1e-11 & 1.0e-11 \\ 1.0e-11 & 9.1e-11 \end{pmatrix}.$$

The diagonal elements are the self-inductances, and off-diagonal entries in the matrix are mutual inductances. The inductance matrices for a *twisted-pair* structure are given below:

$f_H = 10^{16}Hz$

$$\begin{pmatrix} 7.3e-11 & 7.6e-17 \\ 7.8e-17 & 7.4e-11 \end{pmatrix}$$

$f_L = 10^6Hz$

$$\begin{pmatrix} 8.9e-11 & 1.0e-16 \\ 1.1e-16 & 9.1e-11 \end{pmatrix}.$$

The mutual inductances for the twisted-pair structure are about 5 orders of magnitude smaller than the corresponding mutual inductances of the normal un-twisted structure. For all practical purposes, the mutual inductance between signals 1 and 2 is negligible. We also observe that the matrix is not symmetric, i.e, there is a slight discrepancy between L_{12} and L_{21}. The difference may have arisen from numerical errors.

4. TWISTED-BUNDLE STRUCTURE

In this section, we generalize the simple twisted-pair structure such that we can minimize the coupling inductances within a multiple-signal bus that has more than two signal lines. As in the twisted-pair structure, we want to create for each current loop, a complementary and opposite current loop such that the resultant magnetic flux linkage in the current loop of a net of interest is zero.

Figure 2 shows a multiple-bit bus with six signal lines and two ground lines. Here, we assume that the top three signal lines of the 6-bit bus share the ground line labeled 0 as their current return

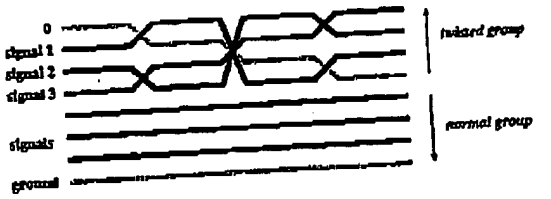

Figure 2: Multiple-signal bus in a twisted-bundle structure.

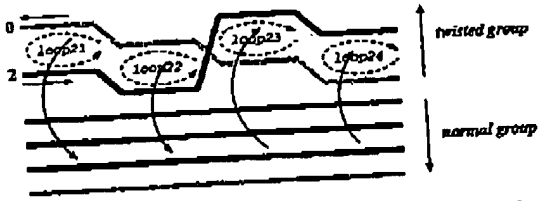

Figure 3: Current loops due to signal line 2 and ground line 0.

paths. The bottom three signal lines share the bottom ground line as their return paths. In the twisted-pair structure, the top signal line and the top ground line are twisted to produce the complementary and opposite current loops. In Figure 2, we twist a *bundle* of the top three signal lines 1, 2, and 3 with the ground line 0, while keeping the bottom three signal lines normal or un-twisted. Hence, we call such a layout structure a *twisted-bundle*, and refer to the group of nets (signal lines and the ground line) that are twisted the *twisted group*. The other group of nets that are not twisted is called the *normal group*.

In the twisted-bundle structure shown in Figure 2, there are four routing regions of equal length in the twisted group. Every signal net in the twisted group goes through the four regions and forms four different loops with the ground line 0. In order to eliminate the mutual inductance, two of the four current loops must form a pair of complementary but opposite loops that are of the same size and of the same distance to the normal group. So do the remaining two current loops. To generate pairs of complementary but opposite loops such that each pair is of the same distance to the normal group, we have to re-order the nets in different routing regions.

Figure 3 illustrates the loops formed by signal 2 and the return path in the four regions. In this example, $loop_{21}$ and $loop_{23}$ cancel each other in the flux linkage of any loop in the normal group, because they are complementary and opposite current loops of the same size, and of the same distance from any loop in the normal group. So do $loop_{22}$ and $loop_{24}$. Hence, the total flux linkage caused by signal 2 (and its return path 0) to any loop in the normal group is equal to zero. Therefore, the mutual inductance between signal 2 and any signal line in the normal group is zero. We can draw similar conclusions for signals 1 and 3.

4.1 Synthesis of Twisted-Bundle

The basic idea of the twisted-bundle structure is to eliminate the mutual inductances, through intelligent net reordering in different routing regions such that the magnetic flux linkages related to one signal-ground pair in different regions cancel each other in the current loop of a net of interest. As the number of the nets in the normal group does not affect the results, the key issue here is the synthesis of the routing pattern in a twisted group.

The order in which the signal nets appear in the twisted bundle defines a *routing matrix*. In a routing matrix, a column represents a routing region in which the net order remains unchanged. For example, the twisted group in Figure 2 corresponds to the following routing matrix:

$$\begin{pmatrix} 0 & 1 & 2 & 3 \\ 1 & 0 & 3 & 2 \\ 2 & 3 & 0 & 1 \\ 3 & 2 & 1 & 0 \end{pmatrix}.$$

In the remainder of this section, we assume that the ground line is labeled 0. We further assume that there are N signal nets labeled 1 through N in the twisted group to be routed. Before we present a systematic approach for synthesizing the routing matrix, we state two observations. First, for the signal nets to be completely routable, each column should be a permutation. Second, in order to generate complementary and opposite current loops, for every signal-ground pair at column x with the signal net, say l, at row y and the ground line 0 at row z, there must exist a column in the matrix such that l is at row z, and 0 at row y. The second observation has two implications:

- There must be at least $(N+1)$ columns in the routing matrix.
- The ground net 0 must appear in all rows in the routing matrix.

We shall now consider the synthesis of a twisted-bundle structure with a odd number of signal nets (i.e., N is odd) and a shared, common ground line. We shall use $N = 7$ to illustrate the idea before presenting the construction of the routing matrix for $N = 2n-1$. A twisted-bundle routing matrix for $N = 7$ is given below:

$$\begin{pmatrix} 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 \\ 1 & 0 & 3 & 4 & 5 & 6 & 7 & 2 \\ 2 & 3 & 0 & 5 & 6 & 7 & 1 & 4 \\ 3 & 4 & 5 & 0 & 7 & 1 & 2 & 6 \\ 4 & 5 & 6 & 7 & 0 & 2 & 3 & 1 \\ 5 & 6 & 7 & 1 & 2 & 0 & 4 & 3 \\ 6 & 7 & 1 & 2 & 3 & 4 & 0 & 5 \\ 7 & 2 & 4 & 6 & 1 & 3 & 5 & 0 \end{pmatrix}$$

For simplicity, we construct the matrix such that the diagonal entries are 0. As a result, the second observation that we stated earlier implies that we should construct a symmetric routing matrix with $(7+1) = 8$ columns if at all possible. To fill in the remaining entries of the matrix, we perform the following tasks:

1. Fill in the first column with $C_1 = [7\,1\,2\,3\,4\,5\,6]^T$ except for the first entry, which is already filled with 0. Displace 7 to the last entry in the column.
2. Perform on $C_1 = [7\,1\,2\,3\,4\,5\,6]^T$ a cyclic shift-up-by-one to obtain $C_2 = [1\,2\,3\,4\,5\,6\,7]^T$.
3. Fill in the second column with C_2 except for the second entry, which is already filled with 0. Displace 2 to the last entry in the column.

In general, we perform on C_i a cyclic shift-up-by-one to obtain C_{i+1}; fill in column $i+1$; and displace the $(i+1)$-th entry in C_{i+1} to the last entry in column $i+1$. We iterate that process until we reach the 8-th column. By symmetry, we can simply transpose the 8-th row to form the routing matrix given above. Following such a construction, we can synthesize the routing matrix for any odd number ($N = 2n-1$) of nets (see Figure 4).

Can we apply such construction rules for even number ($N = 2n$) of signal nets? Observe that in the last row of the routing matrix,

$$\begin{pmatrix}
0 & 1 & 2 & 3 & 4 & \cdots & \cdots & 2n-3 & 2n-2 & 2n-1 \\
1 & 0 & 3 & 4 & \cdots & \cdots & 2n-3 & 2n-2 & 2n-1 & 2 \\
2 & 3 & 0 & \cdots & \cdots & 2n-3 & 2n-2 & 2n-1 & 1 & 4 \\
3 & 4 & \cdots & \cdots & 2n-3 & 2n-2 & 2n-1 & 1 & 2 & \cdots \\
4 & \cdots & \cdots & 2n-3 & 0 & 2n-1 & 1 & 2 & 3 & 2n-2 \\
\cdots & \cdots & 2n-3 & 2n-2 & 2n-1 & 0 & 2 & 3 & 4 & 1 \\
\cdots & 2n-3 & 2n-2 & 2n-1 & 1 & 2 & 0 & 4 & \cdots & 3 \\
2n-3 & 2n-2 & 2n-1 & 1 & 2 & 3 & 4 & \cdots & \cdots & \cdots \\
2n-2 & 2n-1 & 1 & 2 & 3 & 4 & \cdots & \cdots & 0 & 2n-3 \\
2n-1 & 2 & 4 & \cdots & 2n-2 & 1 & 3 & \cdots & 2n-3 & 0
\end{pmatrix}$$

Figure 4: Routing matrix for $N = 2n-1$ signal nets and a common ground line in a twisted group.

the net number in column i is always larger than the net number in column $(i-1)$ by 2 (modulo N). That is because we perform a cyclic shift-up-by-one operation for the vector C_{i-1} and a shift down-by-one for the ground line 0. When $N = 2n-1$, the last row actually forms a permutation. Therefore, we can fill in the last column easily.

When $N = 2n$, however, the last row does not form a permutation. The first eight columns of the following routing matrix are obtained for $N = 8$ signal nets by applying the construction rules outlined earlier:

$$\begin{pmatrix}
0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 0 & 2 & 1 & 4 & 3 & 6 & 5 & 8 & 7 \\
1 & 0 & 3 & 4 & 5 & 6 & 7 & 8 & 2 & 2 & 0 & 4 & 3 & 6 & 5 & 8 & 7 & 1 \\
2 & 3 & 0 & 5 & 6 & 7 & 8 & 1 & 4 & 1 & 4 & 0 & 6 & 5 & 8 & 7 & 2 & 3 \\
3 & 4 & 5 & 0 & 7 & 8 & 1 & 2 & 6 & 4 & 3 & 6 & 0 & 8 & 7 & 2 & 1 & 5 \\
4 & 5 & 6 & 7 & 0 & 1 & 2 & 3 & 7 & 3 & 6 & 5 & 8 & 0 & 2 & 1 & 4 & 8 \\
5 & 6 & 7 & 8 & 1 & 0 & 3 & 4 & 1 & 6 & 5 & 8 & 7 & 2 & 0 & 4 & 3 & 2 \\
6 & 7 & 8 & 1 & 2 & 3 & 0 & 5 & 3 & 5 & 8 & 7 & 2 & 1 & 4 & 0 & 6 & 4 \\
7 & 8 & 1 & 2 & 3 & 4 & 5 & 0 & 5 & 8 & 7 & 2 & 1 & 4 & 3 & 6 & 0 & 6 \\
8 & 2 & 4 & 6 & 8 & 2 & 4 & 6 & 0 & 7 & 1 & 3 & 5 & 7 & 1 & 3 & 5 & 0
\end{pmatrix}$$

It is easy to deduce that in the left half of the preceding matrix, every even-numbered signal net appear twice in the last row as follows:

$$[2n\ 2\ 4\ \ldots\ 2n-2\ 2n\ 2\ 4\ \ldots\ 2n-2\ 0].$$

In order to maintain as much symmetry as possible, we transpose the first $N/2$ entries of the last row to the first $N/2$ entries of the $(N+1)$-th column. For the remaining $N/2$ entries of the $(N+1)$-th column, we use the vector $[2n-1\ 1\ 3\ \ldots\ 2n-3]^T$, in order to make every column a permutation. Therefore, only $N/2$ entries in the last row and $N/2$ entries in the last column do not satisfy the requirement that they have complementary and opposite current loops at the distances from the normal group. To overcome that, we construct a right routing matrix to provide those complementary and opposite current loops (see the routing matrix for $N = 8$).

The most direct approach is to generate as the bottom row for the right routing matrix the following pattern:

$$[2n-1\ 1\ 3\ \ldots\ 2n-3\ 2n-1\ 1\ 3\ \ldots\ 2n-3\ 0].$$

This can be achieved easily by taking C_1 in the left routing matrix, and swapping 1 with 2, 3 with 4, and in general $2i-1$ with $2i$. $C_1' = [2\ 1\ 4\ 3\ \ldots\ 2n\ 2n-1]^T$ is the resultant vector. We can apply the same construction as before to obtain the right routing matrix.

Note that the routing matrix is not unique. An alternative routing matrix can be obtained by simply permuting the columns in the original one.

4.2 Caveats

The twisted-bundle structure can significantly eliminate the coupling inductances between signal nets in the twisted group and the normal group if the assumptions that every signal net in a group share a common return path, and there is a return path for each group hold. If these assumptions are not valid, then the structure may fail to eliminate the mutual inductances between two groups, or can only eliminate a portion of the mutual inductance. For the top few signal nets in the normal group, for example, they are equally close to the ground lines above and below them. In this case, current in these signal nets may return through the upper ground line. Nonetheless, for nets in the bottom half of the normal group, they are more likely to use only the lower return path. Again, we assume that quiet or opposite-switching neighboring nets are not ideal return paths because the current would have to go through highly resistive devices.

The mutual inductances between two groups are significantly reduced. It is natural for one to ask the following question: within a group (be it the twisted group or the normal group), is it possible to reduce the mutual inductances for signal nets within one group as we do between two groups? The answer is no. As long as two signal nets share one common return path, the mutual inductance can not be reduced by net reordering. We prove this in the following.

There are four relative positions for two signal lines and the common ground line as illustrated in Figure 5. We examine the inductive noise induced by signal 1 on signal line 2. We assume that the current in signal 1 flows from the left to right, and that it is increasing. The directions of the magnetic flux produced are depicted by the round direction symbols in Figure 5. By the Faraday's law, the inductive noise (emf) on signal 2 will try to counteract the change of magnetic flux in the loop formed by signal 2 and the ground. Therefore, in each of the four cases, the direction of this induced voltage drop on signal 2 is from the right to left, as shown in Figure 5. Hence, the mutual inductance cannot be eliminated.

5. EXPERIMENTAL RESULTS

Based on the twisted-bundle structure, a 16-bit bus is designed, as shown in Figure 6. The 16 signals are divided into four groups, with 4 signals in each group. Twisted groups and normal groups are alternated. To join the adjacent routing regions in the twisted groups, another metal layer is used. Figure 7 shows part of the stick diagram of the twisted group. In a normal group, the ground line is in the middle, sandwiched between two signal lines above it and two below it.

To show the advantage of the twisted-bundle structure, a traditional 16-bit bus, which consists of 4 normal groups, is constructed for comparison. We refer to it as the normal structure. The inductance matrix for the two kinds of buses are shown below. Only the first four columns of the 16x16 matrix are shown. Rows 1 through 4 are for nets within the first group; the rest are the coupling inductance between nets in the first group and the remaining groups. We assume that the buses are $2mm$ long. For all the metal wires, the thickness is $1\mu m$, and the width and spacing are both assumed

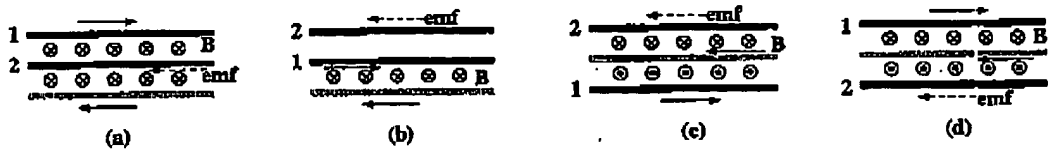

Figure 5: Two signals sharing a common return path.

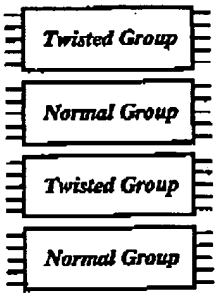

Figure 6: A 16-bit signal bus in a twisted-bundle structure.

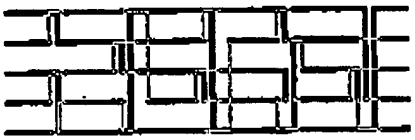

Figure 7: Stick diagram of the layout for a twisted group (not drawn to scale).

to be $1\mu m$. The spacing between the two metal layers is $1\mu m$. The inductance matrix of the twisted-bundle structure is given below:

$$\begin{pmatrix} 1.5e-09 & 5.9e-10 & 8.2e-10 & 8.4e-10 \\ 5.9e-10 & 1.5e-09 & 8.4e-10 & 8.2e-10 \\ 8.2e-10 & 8.4e-10 & 1.8e-09 & 1.1e-09 \\ 8.4e-10 & 8.2e-10 & 1.1e-09 & 1.8e-09 \\ 3.6e-13 & 5.2e-13 & 5.4e-13 & 1.0e-12 \\ 2.6e-13 & 3.2e-13 & 1.7e-13 & 3.6e-13 \\ 2.0e-13 & 2.5e-13 & 1.1e-13 & 2.4e-13 \\ 3.6e-13 & 4.4e-13 & 1.9e-13 & 4.1e-13 \\ 1.2e-11 & 8.1e-13 & 9.8e-12 & 9.8e-12 \\ 7.9e-13 & 1.2e-11 & 9.8e-12 & 9.7e-12 \\ 1.1e-11 & 8.7e-12 & 2.7e-11 & 2.1e-11 \\ 8.8e-12 & 1.1e-11 & 2.1e-11 & 2.7e-11 \\ 7.2e-14 & 9.3e-14 & 4.0e-14 & 8.0e-14 \\ 3.3e-14 & 4.3e-14 & 1.9e-14 & 3.7e-14 \\ 2.9e-14 & 3.8e-14 & 1.6e-14 & 3.3e-14 \\ 5.5e-14 & 7.2e-14 & 3.1e-14 & 6.2e-14 \end{pmatrix}$$

Table 1: Input patterns for investigating the noise levels in signal 8.

Wire Index:	0123456789ABCDEF
Pattern 1	0000000f0f000000
Pattern 2	0000ffff0ffff000
Pattern 3	0000fffr0rfff000
Pattern 4	ffffffff0ffffffff
Pattern 5	fffffffr0rffffff

The inductance matrix of the normal structure is given below:

$$\begin{pmatrix} 1.8e-09 & 8.8e-10 & 4.4e-10 & 6.0e-10 \\ 8.8e-10 & 1.2e-09 & 3.2e-10 & 4.4e-10 \\ 4.4e-10 & 3.2e-10 & 1.2e-09 & 8.8e-10 \\ 6.0e-10 & 4.4e-10 & 8.8e-10 & 1.8e-09 \\ 7.0e-11 & 4.2e-11 & 7.3e-11 & 2.3e-10 \\ 2.8e-11 & 1.6e-11 & 2.6e-11 & 7.3e-11 \\ 2.0e-11 & 1.1e-11 & 1.6e-11 & 4.2e-11 \\ 3.4e-11 & 2.0e-11 & 2.8e-11 & 7.0e-11 \\ 1.6e-11 & 9.0e-12 & 1.1e-11 & 2.6e-11 \\ 7.3e-12 & 4.0e-12 & 5.0e-12 & 1.1e-11 \\ 6.1e-12 & 3.3e-12 & 4.0e-12 & 9.0e-12 \\ 1.1e-11 & 6.1e-12 & 7.3e-12 & 1.6e-11 \\ 7.2e-12 & 3.8e-12 & 4.4e-12 & 9.6e-12 \\ 3.3e-12 & 1.8e-12 & 2.0e-12 & 4.4e-12 \\ 2.9e-12 & 1.6e-12 & 1.8e-12 & 3.8e-12 \\ 5.6e-12 & 2.9e-12 & 3.3e-12 & 7.2e-12 \end{pmatrix}$$

As we can see, the mutual inductances between signal nets within the first group are similar in both matrices. The mutual inductances between signal nets in the first twisted group and the two normal groups are about two orders of magnitude smaller than those between corresponding nets in the normal structure. The mutual inductances between the two twisted groups are not zero. As the two groups are separated by a normal group, the distance between them makes the mutual inductances smaller than those in the first group.

We also extract the capacitance and inductance values for different wire lengths, and simulate the resulting RLC networks in SPICE using different input patterns at $1GHz$ and $2GHz$ signal frequencies. Wire lengths are $1mm$, $2mm$ and $4mm$, representing typical top-level global wires between repeaters or gates in high-speed circuits [5]. For all traces, the drivers are $160X$ of the minimum inverter in a representative $0.18\mu m$ CMOS technology with $1.5V$ V_{dd}, and the receivers are $40X$ of the minimum inverter.

Table 1 describes the input patterns used in the simulations. We index the signals in a 16-bit bus from 0 to F. Note that wire 0 here is not the ground wire. In this table, 'r', 'f', and '0' stand for 'rising', 'falling', and 'quiet', respectively. The rise and fall times of the signals are assumed to be one-tenth of the clock period. All

Table 2: Comparison of noise levels between the twisted-bundle and normal structures.

Length (*mm*)	Input Pattern	Noise (*V*)			
		freq=1*GHz*		freq=2*GHz*	
		Twisted	Normal	Twisted	Normal
1	1	0.05	0.17	0.07	0.25
	2	0.23	0.25	0.32	0.40
	3	0.13	0.16	0.18	0.28
	4	0.23	0.26	0.38	0.39
	5	0.12	0.18	0.18	0.28
2	1	0.09	0.36	0.11	0.42
	2	0.38	0.46	0.44	0.55
	3	0.18	0.35	0.23	0.46
	4	0.37	0.47	0.44	0.55
	5	0.18	0.34	0.23	0.48
4	1	0.14	0.55	0.15	0.59
	2	0.51	0.66	0.53	0.67
	3	0.21	0.51	0.23	0.55
	4	0.53	0.66	0.54	0.68
	5	0.23	0.49	0.24	0.55

Table 3: Comparison of maximum delays between the twisted-bundle and normal structures.

Length,freq	Maximum delay (*ns*)		
	Twisted Structure		Normal Structure
	twisted	normal	
1*mm*,1*GHz*	0.040	0.041	0.041
1*mm*,2*GHz*	0.033	0.033	0.034
2*mm*,1*GHz*	0.069	0.073	0.072
2*mm*,2*GHz*	0.061	0.067	0.065
4*mm*,1*GHz*	0.140	0.146	0.145
4*mm*,2*GHz*	0.129	0.138	0.137

switching signals switch at the same time. Table 2 shows the noise levels measured at the far end of the victim signal 8. From the simulation results, we observe that the twisted-bundle structure can effectively reduce the coupling noise. For 1*mm* wire, we achieve 4% to 72% noise reduction; for 2*mm* wire, 18% to 76%; and for 4*mm* wire, 20% to 75%. Similar results are obtained when we use input patterns obtained by substituting '1' for '2' and '2' for '1' in the five input patterns listed in Table 1.

The impact of the twisted-bundle structure on signal delay is also investigated. The input patterns are similar to those in Table 1 except that signal 8 is also switching (both high and low) instead of being quiet. Table 3 summarizes the maximum delays found for the twisted-bundle and normal structures. The second and third columns in Table 3 list the maximum delays of nets in the twisted groups and normal groups of the twisted-bundle structure, respectively; the fourth column lists the maximum delays of nets in the normal structure. Although every wire in a twisted group has a longer wire length, a higher resistance, and a higher capacitance than wires in a normal group, the simulation results show that wire twisting has minimal impact on the maximum delays. The maximum delays for twisted wires and normal wires in the twisted-bundle structure do not differ by more than 10%. The differences between the maximum delays of the twisted structure and normal structure are even smaller.

6. CONCLUSION

In this paper, we present the *twisted-bundle* layout structure. Inductance extraction with FastHenry shows the effectiveness of this structure in minimizing mutual inductance. SPICE simulation results also show that it can considerably reduce the coupling noise.

Acknowledgment

We thank Mr. Haoran Wang of Purdue University for his help in preparing this manuscript.

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Docket No.: 42390.P13294

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:
Lyn Mark Elzinga

Application No. 10/040,536

Filed: December 28, 2001

For: INTERCONNECT SWIZZLING FOR CAPACATIVE AND INDUCTIVE NOISE CANCELLATION

Examiner: Vuthe Siek

Art Unit: 2825

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, Fax No. (703) 872-9306 on 6/25/04

Date Lawrence M. Mennemeier

APPELLANT'S BRIEF UNDER 37 CFR § 1.192
IN SUPPORT OF APPELLANT'S APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Mail Stop Appeal Brief-Patents
Commissioner of Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellant hereby submits this Brief in triplicate in support of an appeal from a final decision of the Examiner, in the above-referenced case. Appellant respectfully requests consideration of this appeal by the board of Patent Appeals and Interference for allowance of the above-referenced patent application.

TABLE OF CONTENTS

I. Real Party in Interest

The real party in interest in the present appeal is Intel Corporation of Santa Clara, California, the assignee of the present application.

II. Related Appeals and Interferences

There are no related appeals or interferences to appellant's knowledge that would have a bearing on any decision of the Board of Patent Appeals and Interferences.

III. Status of the Claims

Claims 1-23 and 26-38 are allowed

Claims 24 and 25 stand rejected under 35 USC § 102(b) as allegedly being anticipated by US Patent 5,534,732 (DeBrosse).

IV. Status of Amendments

A preliminary amendment, submitted by appellant on 6/7/2002 was entered. An official response to a first Office Action mailed 7/15/2003 was submitted by appellant on 11/17/2003 and was entered. A Final Office Action was mailed on 1/28/2004. Appellant responded by submitting an amendment and official response after final on 3/23/2004, which was entered and an Advisory Action was mailed 5/4/2004. A Notice of Appeal was transmitted on 4/28/2004, and an appeal ensued.

Accordingly, the claims stand as of the entered amendment of 3/23/2004, and are reproduced in clean form in the Appendix.

V. Summary of the Invention

Appellant's disclosure describes a process to employ swizzling that provides capacitive and inductive noise cancellation on a set of concurrently active signal lines. A positive noise due to a capacitive coupling between an attacker signal line and a near victim signal line is, in part, cancelled by a negative or opposite noise due to an inductive coupling between the attacker signal line and a far victim signal line. A swizzling pattern is set forth whereby signal lines of one segment are reordered to transpose near victim signal lines and far victim signal lines in subsequent segments to facilitate the capacitive and inductive cancellation. The swizzling pattern is selected to further facilitate similar capacitive and inductive noise cancellation among the other signal lines of the set.

In some embodiments, the process continues to employ the swizzling pattern in multiple stages to place each signal line adjacent to every other signal line of the set in some swizzle stage. In some alternative embodiments, swizzling patterns may be selected which place each signal line adjacent to every other signal line of the set in some predetermined number of swizzle stages. Subsequent stages of swizzling provide the set of signal lines with capacitive and inductive noise cancellation in addition to the capacitive and inductive noise cancellations of previous stages. The signal lines are optionally reordered by a final swizzle stage to restore the set's original order. In some embodiments, swizzling patterns may be selected from cyclic swizzle groups such that repeating the swizzling pattern automatically restores the set's original order and/or places each signal line adjacent to other signal lines of the set in a predetermined number of swizzle stages.

In some embodiments, a plurality of S swizzle stages may be inserted to provide capacitive and inductive noise cancellation within a set of N concurrently active signal lines, S being computed for a particular value of N according to the equation:

$$N^2/2 - (2S+3)N/2 + S + 1 = 0.$$

VI. Issues

1. Is claim 24 anticipated by DeBrosse?

2. Is claims 25 anticipated by DeBrosse?

VII. Grouping of Claims (Independent Claims **Bolded**)

For the purposes of this appeal, claims **24** and 25 do not stand or fall together.

Group I: Means for Providing Multiple Capacitive and Inductive Noise Cancellation Stages.

Claim **24**.

Group II: Means for Providing Multiple Capacitive and Inductive Noise Cancellation Stages and Restoring Initial Order.

Claim 25.

VIII. Argument

A. Claim 24 Is Not Anticipated by DeBrosse

Claim 24 stands rejected under 35 USC § 102(b) as allegedly being anticipated by US Patent 5,534,732 (DeBrosse).

The MPEP § 2131 states that:

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Appellant respectfully submits that in the cited reference, each and every element as set forth in the Group I claim is not found, either expressly or inherently described.

Claim 24, for example, sets forth:

24. (Original) An interconnect comprising:
a set of N active signal lines having an initial order;
means for providing the set of signal lines with a first capacitive and inductive noise cancellation; and;
means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation.

The invention of DeBrosse relates to a single crossing region that traverses paired true/complement line conductors such that intra-pair capacitive coupling is avoided and inter-pair capacitive coupling is matched (abstract; col. 2, lines 47-51; Figs 5 and 7-10).

The Final Office Action states (emphasis added):

"DeBrosse et al. teach an interconnection layout comprising a set of N active signal lines having an initial order (as shown in Figure 5 for example); means for providing the set of signal lines with a first capacitive and inductive noise cancellation; and means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation (shown in Figure 5 for example). DeBrosse et al. show capacitive noise cancellation. Since capacitive and inductive parasitics are inherently included in conductive line[s], thus capacitive noise cancellation inherently includes inductive noise cancellation."

Appellant respectfully disagrees. Appellant submits that (1) in the first region of

DeBrosse, the signal lines are in their initial order where DeBrosse states that intra-pair capacitive coupling between true and complement lines is avoided not cancelled (col. 6, lines 1-23; Fig. 5).

Appellant further submits that (2) in the second region of DeBrosse, capacitive coupling between pairs is matched such that a line which was disposed adjacent to a true signal line of a pair in the first region is then disposed adjacent to the complemented signal line of the pair in the second region and vise-versa. For example the signal labeled 2-bar is adjacent to the signals labeled 1-bar and 3 in the first region and then adjacent to their complements labeled 1 and 3-bar in the second region (Fig. 5). Thus, in DeBrosse, the set of signal lines is provided with a single cancellation of the capacitive couplings from the true and complemented signal lines (col. 6, lines 1-27; Fig. 5).

On the other hand, claim 24 sets forth means for providing the set of signal lines with a first capacitive and inductive noise cancellation, and means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation. DeBrosse does not describe, either expressly or inherently, providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation.

Appellant further submits that (3) from the presence of inductive parasitics in line conductors it can not be concluded that capacitive noise cancellation inherently includes inductive noise cancellation.

In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999):

> To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by

persons of ordinary skill." Continental Can Co. v. Monsanto Co. , 948 F.2d 1264, 1268, 20 U.S.P.Q.2d 1746, 1749 (Fed. Cir. 1991).

The existence of inductive parasitics does not make it clear that the missing descriptive matter, "capacitive and inductive noise cancellation," is necessarily present in the technique described in the reference. The examiner does not provide objective evidence or cogent technical reasoning to support the conclusion of inherency. Capacitive coupling is strongly related to the proximity of the signal lines, which is addressed by DeBrosse. On the other hand, for inductive coupling it is not so much the proximity of a signal line to an attacker signal line as it is the surface area of a current loop or current loops formed by the attacker signal line and its closest return path, which is not addressed by DeBrosse. One signal line may be inductively coupled to many or all of the other signal lines and DeBrosse addresses only adjacent signal lines and their paired complement signal lines.

Appellant provides the following article as extrinsic evidence that the missing descriptive matter would not be recognized by one of skill in the art as being necessarily present in the technique described by DeBrosse.

Exhibit A: Guoan Zhong et al., A Twisted-Bundle Layout Structure for Minimizing Inductive Coupling Noise, *International Conference on Computer-Aided Design*, Nov. 5-9, 2000.

Referring to subsection 4.2 titled "Caveats," paragraphs 2 and 3 and Figure 5, the authors address the question of whether it is possible to reduce mutual inductances within a group of signal lines sharing a common return (such as the one shown in Fig. 11 of DeBrosse) by reordering the positions of signal lines within the group. They conclude that it is not.

Finally, appellant submits that (4) DeBrosse should not be considered equivalent

under 35 U.S.C. 112, paragraph six, to the subject matter set forth in claim 24.

The MPEP § 2181 states that:

> When making a determination of patentability under 35 U.S.C 102 or 103, past practice was to interpret a "means or step plus function" limitation by giving it the "broadest reasonable interpretation." Under the PTO's long-standing practice this meant interpreting such a limitation as reading on any prior art means or step which performed the function specified in the claim without regard for whether the prior art means or step was equivalent to the corresponding structure, material or acts described in the specification. However, in Donaldson, the Federal Circuit stated:
>
> Per our holding, the "broadest reasonable interpretation" that an examiner may give means-plus-function language is that statutorily mandated in paragraph six. Accordingly, the PTO may not disregard the structure disclosed in the specification corresponding to such language when rendering a patentability determination.

While appellant intends that the broadest reasonable interpretation should be given to claims 1-23 and 28-38, all of which have been allowed, the means-plus-function form of claim 24 may not be modified by language containing sufficient structure, material or acts for achieving the specified function. Therefore claim 24 should be construed to cover the corresponding structure, material or acts described in the specification and equivalents thereof.

The MPEP § 2181 also states that:

> [U]nless an element performs the identical function specified in the claim, it cannot be an equivalent for the purposes of 35 U.S.C. 112, sixth paragraph. Pennwalt Corp. v. Durand-Wayland, Inc., 833 F.2d 931, 4 USPQ2d 1737 (Fed. Cir. 1987), cert. denied, 484 U.S. 961 (1988).

For example, as described in paragraph [0041] of the specification for the present application, in a process to employ swizzling that may provide capacitive and inductive noise cancellation on a set of signal lines, a positive noise due to a capacitive coupling between an attacker signal line and a first victim signal line is, in part, cancelled by a negative or opposite noise due to an inductive coupling between the attacker signal line and a second victim signal line.

Paragraph [0046] explains a key observation is that by reversing the positions of

the near victim signal line and far victim signal line with respect to the attacker in a subsequent interconnect segment, a partial cancellation of the capacitive and inductive noise voltages may be provided. Therefore, it will be appreciated that a partial cancellation of capacitive and inductive noise may be provided in a subsequent interconnect segment by a swizzling of a set of signal lines.

Paragraph [0049] also explains that typically the inductive noise from one attacker is weaker than the capacitive noise form one attacker. A key observation is that additional swizzling may be used to provide subsequent stages of further capacitive and inductive noise cancellation for the set by balancing the number of signal lines that are near neighbors in subsequent stages.

DeBrosse does not suggest capacitive and inductive noise cancellation as disclosed in appellant's specification or equivalents thereof, but rather shows a technique for avoidance of capacitive coupling between pairs of true/complement line conductors, and capacitive matching between the true/complement line conductors of one pair and those of its neighbor pairs (col. 1, lines 11-15, col. 2, lines 56-67 and col. 3, lines 1-5). DeBrosse admits that his layout is applicable only to interconnection arrays having a plurality of paired true/complement line conductors (col. 3, lines 28-30).

Appellant respectfully submits that a person of ordinary skill in the art would not have recognized an interchangeability of DeBrosse (which relies upon capacitive matching between the true/complement line conductor pairs) and the capacitive and inductive noise cancellation disclosed in appellant's specification (which does not rely upon such characteristics of true/complement line conductors).

Even if capacitive matching between the true/complement line conductors could

be considered equivalent to the capacitive and inductive noise cancellation function set forth in claim 24, DeBrosse performed it in a substantially different way (by alternating the capacitive coupling of true and complement line conductors and requiring twice as many signal lines as the method disclosed in appellant's specification) with a substantially different result (a single crossing region versus repeatedly swizzling to balance the number of signal lines that are near neighbors for subsequent capacitive and inductive noise cancellation).

DeBrosse does not expressly or inherently describe equivalent means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation. DeBrosse shows a technique including, "forming a single crossing region including crossing the line conductors of each pair once;" (col. 3, lines 13-15). DeBrosse discloses reordering the signal lines only once (col. 3, lines 22-24 and col. 7, lines 63 through col. 8, line 2). Even DeBrosse's title, "Single Twist Layout and Method for Paired Line Conductors of Integrated Circuits," admits the nonequivalence of the prior art element of DeBrosse for allegedly performing the function set forth in claim 24.

Accordingly in light of the argument presented above, appellant respectfully submits that independent claim 24 is not anticipated by DeBrosse.

B. Claim 25 Is Not Anticipated by DeBrosse

Claim 25 stands rejected under 35 USC § 102(b) as allegedly being anticipated by US Patent 5,534,732 (DeBrosse).

In accordance with the arguments presented above with regard to the patentability of claim 24, appellant believes that claim 25 is patentable, first, for including all of the limitations of claim 24, and additionally for the reasons described below.

The MPEP § 2131 states that:

> "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Appellant respectfully submits that in the cited reference, each and every element as set forth in the Group II claim is not found, either expressly or inherently described in as complete detail as is contained in the claim.

Claim 25, for example, sets forth:

> 25. (Original) The interconnect of Claim 24 further comprising:
> means for restoring the initial order of the set of signal lines.

As stated above, the invention of DeBrosse relates to a single crossing region that traverses paired true/complement line conductors such that intra-pair capacitive coupling is avoided and inter-pair capacitive coupling is matched (abstract; col. 2, lines 47-51). Clearly, the initial order of the set of signal lines is not restored by the single crossing region of DeBrosse (see for example Figs 5 and 7-10).

The Final Office Action states:

> "DeBrosse et al. teach that signal lines in the crossing region are reordered in the third region in order to obtain initial signal lines in the first region or as original signal lines configuration in initial stage, where the signal lines are substantially parallel (Please se Figs. 5, 7, 8, 9, 10 and 11)."

Appellant respectfully disagrees. Appellant submits that (1) in the first region of

DeBrosse, the signal lines are in their initial order and that initial order is not restored by any means.

Referring to Figure 5, for example, DeBrosse states that in the first region line conductor 1 is disposed adjacent to line conductor 2 and line conductor 1-bar is disposed adjacent to line conductor 2-bar (col. 6, lines 1-6). In contrast, opposite the crossing region, line conductor 1 is disposed adjacent to line conductor 2-bar and line conductor 2 is disposed adjacent to line conductor 3-bar, which is not the same order as their initial order (col. 6, lines 7-13). DeBrosse refers to the pattern applied to initially ordered lines 1, 2, 1-bar, and 2-bar respectively as "down 1," "down 3," "up 3," and "up 1," (col. 6, lines 16-17).

Further, as stated above with regard to claim 24, the means-plus-function form of claim 25 may not be modified by language containing sufficient structure, material or acts for achieving the specified function. Therefore claim 25 should be construed to cover the corresponding structure, material or acts described in the specification and equivalents thereof.

Appellant submits that (2) DeBrosse should not be considered equivalent under 35 U.S.C. 112, paragraph six, to the subject matter set forth in claim 25.

For example, as described in paragraphs [0094] and [0095] of the specification for the present application with reference to Figure 10, it will be appreciated that repeated compositions of c and d generate swizzle groups with respect to an initial order {1,2,3,4,5,6,7,8} as follows:

$$c^1 = \{7,4,1,3,6,8,5,2\}, \quad d^1 = \{2,4,1,6,3,8,5,7\},$$

$$c^2 = \{5,3,7,1,8,2,6,4\}, \quad d^2 = \{4,6,2,8,1,7,3,5\},$$

$c^3 = \{6,1,5,7,2,4,8,3\}$, $d^3 = \{6,8,4,7,2,5,1,3\}$,

$c^4 = \{8,7,6,5,4,3,2,1\}$, $d^4 = \{8,7,6,5,4,3,2,1\}$,

$c^5 = \{2,5,8,6,3,1,4,7\}$, $d^5 = \{7,5,8,3,6,1,4,2\}$,

$c^6 = \{4,6,2,8,1,7,3,5\}$, $d^6 = \{5,3,7,1,8,2,6,4\}$,

$c^7 = \{3,8,4,2,7,5,1,6\}$, $d^7 = \{3,1,5,2,7,4,8,6\}$,

$c^8 = \{1,2,3,4,5,6,7,8\}$, $d^8 = \{1,2,3,4,5,6,7,8\}$.

It will be further appreciated that a swizzling pattern given by c^1, c^1, c^1, c^5, may be employed using swizzling 1041 repeatedly and optionally restoring the initial order of the set using swizzling 1045.

Similarly, Figures 4a-b, 10a-c, 11b, and 13a-d illustrate alternative embodiments where the initial order of a set of signal lines may be restored by swizzling patterns which may be conveniently selected from swizzle groups.

DeBrosse does not expressly or inherently describe equivalent means for restoring the initial order of the set of signal lines. The techniques of DeBrosse use a single crossing region crossing the line conductors of each pair only once and reordering the signal lines exactly once (col. 3, lines 13-24 and col. 7, lines 63 through col. 8, line 2).

Appellant respectfully submits that a person of ordinary skill in the art would not have recognized an interchangeability of the single crossing region of DeBrosse and the swizzling patterns disclosed in appellant's specification for restoring the initial order of the set of signal lines.

Additionally, appellant believes that since the single crossing region of DeBrosse performs a substantially different function (matching true/complement signal line pairs) in a substantially different way (reordering the signal lines exactly once), it is not

equivalent for allegedly performing the function of restoring the initial order of the set of signal lines set forth in claim 25.

Accordingly in light of the argument presented above, appellant respectfully submits that dependent claim 25 is not anticipated by DeBrosse.

Conclusion

Appellant submits that all claims now pending are in condition for allowance. Such action is earnestly solicited at the earliest possible date. If there is a deficiency in fees, please charge our Deposit Acct. No. 02-2666.

Respectfully submitted,

Date: 6/25/2004

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IX. Appendix A: Claims Allowed and Involved in Appeal (Clean Copy)

1. (Original) A method comprising:

swizzling a set of N concurrently active signal lines into a first order to provide a first stage of capacitive and inductive noise cancellation for a first plurality of signal lines of the set; and

swizzling the set of N concurrently active signal lines again into a second order different from the first order to provide a second stage of further capacitive and inductive noise cancellation for the first plurality of signal lines of the set.

2. (Original) The method of Claim 1 wherein a first signal line of the set is adjacent to a first subset of the set of N concurrently active signal lines in the first stage and swizzling the set of N concurrently active signal lines again places the first signal line adjacent to a second subset of the set of N concurrently active signal lines in the second stage, the first subset and the second subset being disjoint.

3. (Original) The method of Claim 2 wherein the first signal line of the set is adjacent to a third subset of the set of signal lines in an initial order of the set of N concurrently active signal lines and swizzling the set of signal lines places the first signal line adjacent to the first subset of signal lines in the first stage, the first subset and the third subset being disjoint.

4. (Original) The method of Claim 1 wherein the set of N concurrently active signal lines have a substantially common origin and a substantially common destination.

5. (Original) The method of Claim 1 wherein swizzling the set of N concurrently active signal lines comprises reordering N signal lines for concurrently carrying N bits of information in substantially parallel signal tracks on a substantially planar substrate by

routing each of a second plurality of said N signal lines from a corresponding pre-swizzling signal track directly to a corresponding post-swizzling signal track, optionally via a substantially parallel planar layer.

6. (Original) The method of Claim 5 wherein each swizzling of the set of N concurrently active signal lines is accomplished by inserting a single swizzle cell.

7. (Original) The method of Claim 1 comprising swizzling the set of N concurrently active signal lines to provide S stages of capacitive and inductive noise cancellation and optionally providing an additional stage to restore an initial order of the set, wherein each of the N concurrently active signal lines of the set is placed adjacent to every other signal line of the set in some stage of the S stages, S being computed from N according to the equation:

$$N^2/2 - (2S+3)N/2 + S + 1 = 0.$$

8. (Original) An article of manufacture comprising

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the method of Claim 7.

9. (Original) An article of manufacture comprising

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the method of Claim 6.

10. (Original) An article of manufacture comprising

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the method of Claim 3.

11. (Original) An article of manufacture comprising

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the method of Claim 1.

12. (Original) The method of Claim 1 wherein the first stage of capacitive and inductive noise cancellation and the second stage of further capacitive and inductive noise cancellation reduce capacitive and inductive noise due to switching within the set of signal lines.

13. (Original) The method of Claim 1 wherein concurrently active indicates that each of the N signal lines may be switched in a single transmission cycle.

14. (Original) An apparatus comprising:

a set of N signal lines configurable to transmit N bits of information in a transmission cycle, the signal lines being substantially parallel and having a first portion with a first signal line order;

a first swizzle stage of the set of N signal lines having a second portion with a second signal line order, wherein a first signal line of the set is adjacent to a first subset of the N signal lines in said first portion and the first signal line is adjacent to a second subset of the N signal lines in said second portion, the first subset and the second subset being disjoint; and

a second swizzle stage of the set of N signal lines having a third portion with a third signal line order, wherein the first signal line of the set is adjacent to a third subset of the N signal lines in said third portion, the first subset the second subset and the third subset being disjoint.

15. (Original) The apparatus of Claim 14 wherein the set of N signal lines have a substantially common origin and a substantially common destination.

16. (Original) The apparatus of Claim 14 comprising

said set of N signal lines in substantially parallel signal tracks on a substantially planar substrate;

each of a first plurality of the N signal lines being routed from a corresponding

signal track in the first portion, according to the first signal line order, directly to a corresponding signal track in the second portion, according to the second signal line order, optionally via one or more substantially parallel planar layers; and

each of a second plurality of the N signal lines being routed from a corresponding signal track in the second portion, according to the second signal line order, directly to a corresponding signal track in the third portion, according to the third signal line order, optionally via the one or more substantially parallel planar layers.

17. (Original) The apparatus of Claim 14 wherein the first swizzle stage of the set of N lines comprises a swizzle cell coupling the first portion with the second portion.

18. (Original) The apparatus of Claim 17 wherein the second swizzle stage of the set of N lines comprises a swizzle cell coupling the second portion with the third portion.

19. (Original) The apparatus of Claim 14 comprising

a plurality of S swizzle stages to provide capacitive and inductive noise cancellation within the set of N signal lines, wherein each of the N signal lines of the set is placed adjacent to every other signal line of the set in some swizzle stage of the S swizzle stages, S being computed for a particular value of N according to the equation, $N^2/2 - (2S+3)N/2 + S + 1 = 0$; and

an optional final stage to restore an initial order for the set of N signal lines.

20. (Original) The apparatus of Claim 14 wherein the third portion of the second swizzle stage places no signal line, of the set of N signal lines, adjacent to one of the same signal lines that they are adjacent to in the second portion of the first swizzle stage.

21. (Original) The apparatus of Claim 20 wherein the second portion of the first swizzle stage places no signal line, of the set of N signal lines, adjacent to one of the same signal lines that they are adjacent to in the first portion.

22. (Original) The apparatus of Claim 21 wherein the third portion of the second swizzle stage places no signal line, of the set of N signal lines, adjacent to one of the same signal lines that they are adjacent to in the first portion.

23. (Original) The apparatus of Claim 14 comprising

a first swizzle cell to reorder the set of N signal lines from the first signal line order into the second signal line order;

a second swizzle cell to reorder the set of N signal lines from the second signal line order into the third signal line order; and

an optional third swizzle cell to restore an initial order for the set of N signal lines.

24. (Original) An interconnect comprising:

a set of N active signal lines having an initial order;

means for providing the set of signal lines with a first capacitive and inductive noise cancellation; and;

means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation.

25. (Original) The interconnect of Claim 24 further comprising:

means for restoring the initial order of the set of signal lines.

26. (Previously Amended) An interconnect comprising:

a set of N active signal lines having an initial order;

means for providing the set of signal lines with a first capacitive and inductive noise cancellation;

means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation; and

means for restoring the initial order of the set of signal lines, wherein the means for restoring the initial order of the set of signal lines provides the set of signal lines with a third capacitive and inductive noise cancellation in addition to the first and second

capacitive and inductive noise cancellations.

27. (Original) The interconnect of Claim 26 wherein the set of signal lines contains an even number of signal lines.

28. (Original) An article of manufacture comprising:

a machine-accessible medium including data that, when accessed by a machine, cause the machine to:

insert a first swizzle stage to provide a set of N concurrently active signal lines having a first signal line order, with a second signal line order, where in the first signal line order, a first signal line of the set is adjacent to a first subset of the N signal lines and in the second signal line order the first signal line is adjacent to a second subset of the N signal lines, the first subset and the second subset having no signal lines in common; and

insert a second swizzle stage to provide the set of N concurrently switched signal lines with a third signal line order, where in the third signal line order the first signal line is adjacent to a third subset of the N signal lines, the first subset, the second subset and the third subset having no signal lines in common.

29. (Original) The article of manufacture of Claim 28 wherein the second signal line order of the first swizzle stage provides a capacitive and inductive noise cancellation by placing the first signal line adjacent to the second subset of the N signal lines.

30. (Original) The article of manufacture of Claim 29 wherein the third signal line order of the second swizzle stage provides an additional capacitive and inductive noise cancellation by placing the first signal line adjacent to the third subset of the N signal lines.

31. (Original) The article of manufacture of Claim 30 wherein the first capacitive and inductive noise cancellation and the additional capacitive and inductive noise cancellation reduce capacitive and inductive noise due to switching within the set of N concurrently

active signal lines.

32. (Original) The article of manufacture of Claim 28 wherein the third signal line order of the second swizzle stage places no signal line, of the set of N concurrently active signal lines, adjacent to one of the same signal lines that they are adjacent to in the second signal line order of the first swizzle stage.

33. (Original) The article of manufacture of Claim 32 wherein second signal line order of the first swizzle stage places no signal line, of the set of N concurrently active signal lines, adjacent to one of the same signal lines that they are adjacent to in the first signal line order.

34. (Original) The article of manufacture of Claim 33 further including data that when accessed by the machine, cause the machine to:

insert a third swizzle stage to restore the set of N concurrently active signal lines to their original order.

35. (Original) The article of manufacture of Claim 28 wherein concurrently active indicates that each of the N signal lines may be switched in a transmission cycle.

36. (Original) The article of manufacture of Claim 28 further including data that when accessed by the machine, cause the machine to:

insert a plurality of S swizzle stages to provide capacitive and inductive noise cancellation within the set of N concurrently active signal lines, wherein each of the N signal lines of the set is placed adjacent to every other signal line of the set in some swizzle stage of the S swizzle stages, S being computed for a particular value of N according to the equation

$$N^2/2 - (2S+3)N/2 + S + 1 = 0; \text{ and}$$

insert an optional swizzle to restore an initial order for the set of N concurrently active signal lines.

37. (Original) An apparatus comprising:

a set of N concurrently active signal lines, the signal lines being substantially parallel and having a first signal line order;

a plurality of swizzle cells linking segments of the set of N concurrently active signal lines, the plurality of swizzle cells transposing near victim signal lines and far victim signal lines in subsequent segments to facilitate capacitive and inductive noise cancellation within the set of N concurrently active signal lines; and

an optional swizzle cell to restore an initial order for the set of N concurrently active signal lines.

38. (Original) The apparatus of Claim 37 wherein concurrently active indicates that each of the N signal lines may be switched in a single transmission cycle.

Exhibit A

Guoan Zhong et al., A Twisted-Bundle Layout Structure for Minimizing Inductive Coupling Noise, *International Conference on Computer-Aided Design*, Nov. 5-9, 2000.

A Twisted-Bundle Layout Structure for Minimizing Inductive Coupling Noise*

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ABSTRACT

In this paper, we propose a novel *twisted-bundle* layout structure for minimizing inductive coupling noise. In this structure, we create several routing regions and re-order the routing of nets in each of these routing regions. The purpose is to create complementary and opposite current loops in the twisted-bundle layout structure, such that the magnetic fluxes arising from any signal net within a *twisted group* cancel each other in the current loop of a net of interest. The effectiveness of the twisted-bundle structure in minimizing coupling inductance has been verified by the application of FastHenry extraction on a 16-bit bus structure. We achieve about two orders of magnitude reduction in inductive coupling. SPICE simulations also show that the 16-bit twisted-bundle bus structure is able to maintain high signal integrity at high frequency of operation.

1. INTRODUCTION

Continued scaling of semiconductor technology has brought the issues of interconnect-limited designs to the forefront. The International Technology Roadmap for Semiconductor (ITRS) [1] forecasts that as the VLSI technology advances towards giga-Hertz on-chip frequency and system-level integration on larger die size, self- and coupling-inductances are becoming dominant factors in determining signal delay and signal integrity.

Ref. [16] gave an extensive survey of various noise sources in circuit design. Predominantly, existing studies focused on cross-talk noise due to capacitive coupling. Due to the short range effect of capacitive coupling, techniques such as shielding, net ordering or track permutation have proved to be effective in minimizing capacitive cross-talk noise [6; 17].

On the other hand, inductive effects have a long range effect because they arise from the electromagnetic phenomenon of magnetic flux linking current loops. As a result, inductive noise has a much wider spatial effect than that of a capacitive noise. For this reason, it makes the worst case situation in a circuit much harder to predict. Many of the existing studies that dealt with on-chip inductive effects focused primarily on the modeling and extraction of on-chip interconnect inductance. In [15], loop inductance was calculated in terms of partial inductances defined for wire segments. The Partial Element Equivalent Circuit (PEEC) model was widely used to analyze on-chip inductance [7; 14; 4]. In [9], frequency dependent inductance and resistance were computed based on the magnetoquasistatic assumption, and in [10], a simple layout rule-based method was used to speed up the computation.

*This research is supported in part by SRC (99-TJ-689), NSF (CAREER Award CCR-9984553), and a grant from Intel Corporation.

A few recent studies have reported success in minimizing the undesirable inductive effects. In recent Alpha chip designs [2], on-chip inductance was limited by sandwiching lines with high current density between isolating metal planes. In [11], the wiring overhead was reduced by using a interdigitated layout structure, in which a wide wire was split into many lines, interspersed with ground lines. These techniques, however, considered only self-inductance. In [8], inductive coupling noise was reduced by shield insertion and net ordering.

In this paper, we propose a novel *twisted-bundle* layout structure for minimizing inductive coupling noise. By creating complementary and opposite current loops in the layout structure, we achieve two orders of magnitude reduction in inductive coupling. The abilities of the twisted-bundle structure in minimizing coupling inductance and maintaining high signal integrity have been verified by the applications of FastHenry extraction and SPICE simulations on a 16-bit bus structure.

The rest of the paper is organized as follows. In Section 2, preliminaries regarding inductive coupling are explained. In Section 3, we introduce a twisted-pair layout structure, upon which the twisted-bundle structure is based. In Section 4, we present the novel twisted-bundle structure and a systematic approach for synthesizing such a structure. In Section 5, we apply this structure to a 16-bit bus design and compare it with the "traditional" design based on the parasitic parameters extracted by FastHenry and the simulation results by SPICE. Finally, we conclude in Section 6.

2. PRELIMINARIES

Mutual inductances, as well as self inductance, are electromagnetic phenomena that arises from current loops [12; 13]. The inductances for a system of N loops are defined as:

$$L_{ij} = \frac{\Psi_{ij}}{I_j}, \tag{1}$$

where Ψ_{ij} is the magnetic flux in loop i due to a current I_j in loop j. L_{ii} represents the self inductance of loop i, whereas $L_{ij}(i \neq j)$ represents the mutual inductance between loops i and j.

According to the Faraday's law, the mutual inductance can be calculated by finding the magnetic flux linking one loop related to per unit of current in the other loop:

$$M = L_{ij} = \iint_{S_i} \vec{B} \cdot d\vec{S}_i \,/\, I_j, \tag{2}$$

where B is the density of the magnetic flux arising from current I_j in loop i and the integration is over the surface of loop i.

On-chip signal nets form loops with their current return paths; these loops determine the inductances as shown in Eqns. (1) and (2). Therefore, in order to accurately calculate the inductances of

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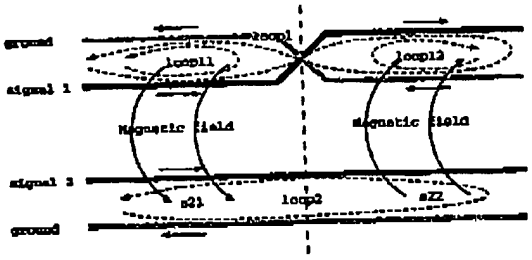

Figure 1: Twisted-pair structure.

on-chip interconnections, it is of critical importance to determine the current return paths of on-chip signal nets. However, it is extremely difficult to find accurate return paths for signal nets, because in the complex interconnection structures that we deal with today, there are several paths through which a current returns [3].

In this work, we assume that all signals use the nearest power/ground line as their return paths [5]. Although quiet or opposite-switching neighboring nets may also serve as return paths, they are not ideal because currents returning from signal wires have to go through devices, which typically have a resistance of several hundred Ohms.

3. TWISTED-PAIR LAYOUT STRUCTURE

From the Faraday's law, there are two possible ways of eliminating the coupling inductance: (i) by creating a magnetic flux that is of an opposite direction; (ii) by eliminating or minimizing the surface area of the second loop. To achieve that, we propose a simple *twisted-pair* layout structure (Figure 1) that is inspired by the twisted-pair wire structure.

As shown in Figure 1, we consider two signal lines in this structure. For each signal line, we assume that there exists a ground line nearby, serving as the signal's dedicated return path. The signal and ground lines are drawn with different shades of gray. Like the twisted-pair wire structure, we intertwine one signal line and its return path at their mid-points such that they are "symmetric" about the mid-points. As the signal and ground lines co-exist on the same metal layer, the physical layout of such a twisted-pair structure involves vias and doglegs.

As indicated in Figure 1, signal lines 1 and 2 form respectively loops $loop_1$ and $loop_2$ with their dedicated return paths. As signal 1 and its return path are twisted, $loop_1$ is divided into two smaller loops: $loop_{11}$ and $loop_{12}$. In quasi-static condition, the current is continuous everywhere along a signal line. Therefore, the two current loops flow in opposite directions, and the magnetic fields caused by $loop_{11}$ and $loop_{12}$ are equal in magnitude, but in opposite directions. According to the Faraday's law in Eqn. (2), the mutual inductance $M = L_{21}$ can be calculated by finding the magnetic flux linking $loop_1$ to $loop_2$:

$$M = \int\int_{s_2} \vec{B} \cdot d\vec{S}_2 \; / \; I_1. \tag{3}$$

As the integration is over the surface of $loop_2$, we divide the surface of loop into two equal parts S_{21} and S_{22} along the mid-line drawn in Figure 1. We rewrite Eqn. (3) as:

$$M = (\int\int_{s_{21}} \vec{B} \cdot d\vec{S}_{21} + \int\int_{s_{22}} \vec{B} \cdot d\vec{S}_{22}) \; / \; I_1. \tag{4}$$

When the lengths of the wires are much larger than the spacing between the wires, the magnetic flux linkage in S_{21} mainly comes from $loop_{11}$, and the magnetic flux linkage in S_{22} is primarily due to $loop_{12}$. As the current directions in $loop_{11}$ and $loop_{12}$ are opposite, the directions of the magnetic fluxes in S_{21} and S_{22} are opposite. Therefore, the two integrations over S_{21} and S_{22} cancel each other:

$$\int\int_{s_{22}} \vec{B} \cdot d\vec{S}_{22} = - \int\int_{s_{21}} \vec{B} \cdot d\vec{S}_{21}; \tag{5}$$

Hence, the mutual inductance between signals 1 and 2 is zero:

$$M = (\int\int_{s_{21}} \vec{B} \cdot d\vec{S}_{21} - \int\int_{s_{22}} \vec{B} \cdot d\vec{S}_{21}) \; / \; I_1 = 0. \tag{6}$$

In fact, $loop_{12}$ also contributes to the magnetic flux linkage in S_{21}. So does $loop_{11}$ to S_{22}. However, their contributions are quite insignificant, as these two components of magnetic flux also cancel each other in the integration. We can similarly argue that L_{12} is zero because the surfaces of the two loops $loop_{11}$ and $loop_{12}$ actually "sum" to zero.

All the preceding discussions are based on the assumption that the current in a signal line is continuous everywhere. However, this assumption is not valid when the wire length is sufficiently long for the transmission line effect to kick in. If parallel termination is adopted at the receiving ends of signal lines, there are no or minimal reflections at the receiving ends. Consequently, noises gathered at the victim nets cancel each other when they reach the receiving ends. Hence, the mutual inductance is still zero.

We use FastHenry [9] to verify the effectiveness of the proposed twisted-pair layout structure in minimizing coupling inductance. The wire width, height, length, and spacing are $1\mu m$, $2\mu m$, $200\mu m$, and $1\mu m$, respectively.

We extract the inductance matrix under two frequencies: a *high* frequency of $f_H = 10^{16} Hz$ and a *low* frequency of $f_L = 10^6 Hz$. The inductance matrices for a *normal* or *un-twisted* structure are given below:

$$f_H = 10^{16} Hz \quad \begin{pmatrix} 7.4e-11 & 6.2e-12 \\ 6.2e-12 & 7.4e-11 \end{pmatrix} \qquad f_L = 10^6 Hz \quad \begin{pmatrix} 9.1e-11 & 1.0e-11 \\ 1.0e-11 & 9.1e-11 \end{pmatrix}.$$

The diagonal elements are the self-inductances, and off-diagonal entries in the matrix are mutual inductances. The inductance matrices for a *twisted-pair* structure are given below:

$$f_H = 10^{16} Hz \quad \begin{pmatrix} 7.3e-11 & 7.6e-17 \\ 7.8e-17 & 7.4e-11 \end{pmatrix} \qquad f_L = 10^6 Hz \quad \begin{pmatrix} 8.9e-11 & 1.0e-16 \\ 1.1e-16 & 9.1e-11 \end{pmatrix}.$$

The mutual inductances for the twisted-pair structure are about 5 orders of magnitude smaller than the corresponding mutual inductances of the normal un-twisted structure. For all practical purposes, the mutual inductance between signals 1 and 2 is negligible. We also observe that the matrix is not symmetric, i.e, there is a slight discrepancy between L_{12} and L_{21}. The difference may have arisen from numerical errors.

4. TWISTED-BUNDLE STRUCTURE

In this section, we generalize the simple twisted-pair structure such that we can minimize the coupling inductances within a multiple-signal bus that has more than two signal lines. As in the twisted-pair structure, we want to create for each current loop, a complementary and opposite current loop such that the resultant magnetic flux linkage in the current loop of a net of interest is zero.

Figure 2 shows a multiple-bit bus with six signal lines and two ground lines. Here, we assume that the top three signal lines of the 6-bit bus share the ground line labeled 0 as their current return

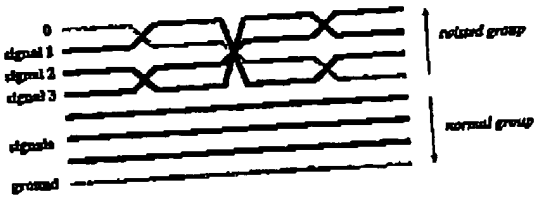

Figure 2: Multiple-signal bus in a twisted-bundle structure.

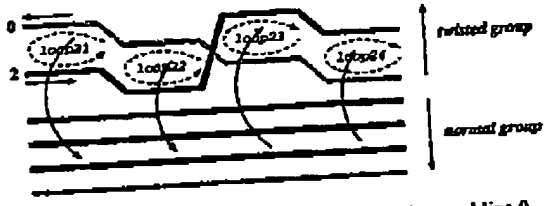

Figure 3: Current loops due to signal line 2 and ground line 0.

paths. The bottom three signal lines share the bottom ground line as their return paths. In the twisted-pair structure, the top signal line and the top ground line are twisted to produce the complementary and opposite current loops. In Figure 2, we twist a *bundle* of the top three signal lines 1, 2, and 3 with the ground line 0, while keeping the bottom three signal lines normal or un-twisted. Hence, we call such a layout structure a *twisted-bundle*, and refer to the group of nets (signal lines and the ground line) that are twisted the *twisted group*. The other group of nets that are not twisted is called the *normal group*.

In the twisted-bundle structure shown in Figure 2, there are four routing regions of equal length in the twisted group. Every signal net in the twisted group goes through the four regions and forms four different loops with the ground line 0. In order to eliminate the mutual inductance, two of the four current loops must form a pair of complementary but opposite loops that are of the same size and of the same distance to the normal group. So do the remaining two current loops. To generate pairs of complementary but opposite loops such that each pair is of the same distance to the normal group, we have to re-order the nets in different routing regions.

Figure 3 illustrates the loops formed by signal 2 and the return path in the four regions. In this example, $loop_{21}$ and $loop_{23}$ cancel each other in the flux linkage of any loop in the normal group, because they are complementary and opposite current loops of the same size, and of the same distance from any loop in the normal group. So do $loop_{22}$ and $loop_{24}$. Hence, the total flux linkage caused by signal 2 (and its return path 0) to any loop in the normal group is equal to zero. Therefore, the mutual inductance between signal 2 and any signal line in the normal group is zero. We can draw similar conclusions for signals 1 and 3.

4.1 Synthesis of Twisted-Bundle

The basic idea of the twisted-bundle structure is to eliminate the mutual inductances, through intelligent net reordering in different routing regions such that the magnetic flux linkages related to one signal-ground pair in different regions cancel each other in the current loop of a net of interest. As the number of the nets in the normal group does not affect the results, the key issue here is the synthesis of the routing pattern in a twisted group.

The order in which the signal nets appear in the twisted bundle defines a *routing matrix*. In a routing matrix, a column represents a routing region in which the net order remains unchanged. For example, the twisted group in Figure 2 corresponds to the following routing matrix:

$$\begin{pmatrix} 0 & 1 & 2 & 3 \\ 1 & 0 & 3 & 2 \\ 2 & 3 & 0 & 1 \\ 3 & 2 & 1 & 0 \end{pmatrix}.$$

In the remainder of this section, we assume that the ground line is labeled 0. We further assume that there are N signal nets labeled 1 through N in the twisted group to be routed. Before we present a systematic approach for synthesizing the routing matrix, we state two observations. First, for the signal nets to be completely routable, each column should be a permutation. Second, in order to generate complementary and opposite current loops, for every signal-ground pair at column x with the signal net, say 1, at row y and the ground line 0 at row z, there must exist a column in the matrix such that 1 is at row z, and 0 at row y. The second observation has two implications:

- There must be at least $(N+1)$ columns in the routing matrix.
- The ground net 0 must appear in all rows in the routing matrix.

We shall now consider the synthesis of a twisted-bundle structure with a odd number of signal nets (i.e., N is odd) and a shared, common ground line. We shall use $N = 7$ to illustrate the idea before presenting the construction of the routing matrix for $N = 2n-1$. A twisted-bundle routing matrix for $N = 7$ is given below:

$$\begin{pmatrix} 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 \\ 1 & 0 & 3 & 4 & 5 & 6 & 7 & 2 \\ 2 & 3 & 0 & 5 & 6 & 7 & 1 & 4 \\ 3 & 4 & 5 & 0 & 7 & 1 & 2 & 6 \\ 4 & 5 & 6 & 7 & 0 & 2 & 3 & 1 \\ 5 & 6 & 7 & 1 & 2 & 0 & 4 & 3 \\ 6 & 7 & 1 & 2 & 3 & 4 & 0 & 5 \\ 7 & 2 & 4 & 6 & 1 & 3 & 5 & 0 \end{pmatrix}$$

For simplicity, we construct the matrix such that the diagonal entries are 0. As a result, the second observation that we stated earlier implies that we should construct a symmetric routing matrix with $(7+1) = 8$ columns if at all possible. To fill in the remaining entries of the matrix, we perform the following tasks:

1. Fill in the first column with $C_1 = [7\,1\,2\,3\,4\,5\,6]^T$ except for the first entry, which is already filled with 0. Displace 7 to the last entry in the column.
2. Perform on $C_1 = [7\,1\,2\,3\,4\,5\,6]^T$ a cyclic shift-up-by-one to obtain $C_2 = [1\,2\,3\,4\,5\,6\,7]^T$.
3. Fill in the second column with C_2 except for the second entry, which is already filled with 0. Displace 2 to the last entry in the column.

In general, we perform on C_i a cyclic shift-up-by-one to obtain C_{i+1}; fill in column $i+1$; and displace the $(i+1)$-th entry in C_{i+1} to the last entry in column $i+1$. We iterate that process until we reach the 8-th column. By symmetry, we can simply transpose the 8-th row to form the routing matrix given above. Following such a construction, we can synthesize the routing matrix for any odd number ($N = 2n-1$) of nets (see Figure 4).

Can we apply such construction rules for even number ($N = 2n$) of signal nets? Observe that in the last row of the routing matrix,

$$\begin{pmatrix}
0 & 1 & 2 & 3 & 4 & \cdots & \cdots & 2n-3 & 2n-2 & 2n-1 \\
1 & 0 & 3 & 4 & \cdots & \cdots & 2n-3 & 2n-2 & 2n-1 & 2 \\
2 & 3 & 0 & \cdots & \cdots & 2n-3 & 2n-2 & 2n-1 & 1 & 4 \\
3 & 4 & \cdots & \cdots & 2n-3 & 2n-2 & 2n-1 & 1 & 2 & \cdots \\
4 & \cdots & \cdots & 2n-3 & 0 & 2n-1 & 1 & 2 & 3 & 2n-2 \\
\cdots & \cdots & 2n-3 & 2n-2 & 2n-1 & 0 & 2 & 3 & 4 & 1 \\
\cdots & 2n-3 & 2n-2 & 2n-1 & 1 & 2 & 0 & 4 & \cdots & 3 \\
2n-3 & 2n-2 & 2n-1 & 1 & 2 & 3 & 4 & \cdots & \cdots & \cdots \\
2n-2 & 2n-1 & 1 & 2 & 3 & 4 & \cdots & \cdots & 0 & 2n-3 \\
2n-1 & 2 & 4 & \cdots & 2n-2 & 1 & 3 & \cdots & 2n-3 & 0
\end{pmatrix}$$

Figure 4: Routing matrix for $N = 2n-1$ signal nets and a common ground line in a twisted group.

the net number in column i is always larger than the net number in column $(i-1)$ by 2 (modulo N). That is because we perform a cyclic shift-up-by-one operation for the vector C_{i-1} and a shift down-by-one for the ground line 0. When $N = 2n-1$, the last row actually forms a permutation. Therefore, we can fill in the last column easily.

When $N = 2n$, however, the last row does not form a permutation. The first eight columns of the following routing matrix are obtained for $N = 8$ signal nets by applying the construction rules outlined earlier:

$$\begin{pmatrix}
0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 0 & 2 & 1 & 4 & 3 & 6 & 5 & 8 & 7 \\
1 & 0 & 3 & 4 & 5 & 6 & 7 & 8 & 2 & 2 & 0 & 4 & 3 & 6 & 5 & 8 & 7 & 1 \\
2 & 3 & 0 & 5 & 6 & 7 & 8 & 1 & 4 & 1 & 4 & 0 & 6 & 5 & 8 & 7 & 2 & 3 \\
3 & 4 & 5 & 0 & 7 & 8 & 1 & 2 & 6 & 4 & 3 & 6 & 0 & 8 & 7 & 2 & 1 & 5 \\
4 & 5 & 6 & 7 & 0 & 1 & 2 & 3 & 7 & 3 & 6 & 5 & 8 & 0 & 2 & 1 & 4 & 8 \\
5 & 6 & 7 & 8 & 1 & 0 & 3 & 4 & 1 & 6 & 5 & 8 & 7 & 2 & 0 & 4 & 3 & 2 \\
6 & 7 & 8 & 1 & 2 & 3 & 0 & 5 & 3 & 5 & 8 & 7 & 2 & 1 & 4 & 0 & 6 & 4 \\
7 & 8 & 1 & 2 & 3 & 4 & 5 & 0 & 5 & 8 & 7 & 2 & 1 & 4 & 3 & 6 & 0 & 6 \\
8 & 2 & 4 & 6 & 8 & 2 & 4 & 6 & 0 & 7 & 1 & 3 & 5 & 7 & 1 & 3 & 5 & 0
\end{pmatrix}$$

It is easy to deduce that in the left half of the preceding matrix, every even-numbered signal net appear twice in the last row as follows:

$$[2n\ 2\ 4\ \ldots\ 2n-2\ 2n\ 2\ 4\ \ldots\ 2n-2\ 0].$$

In order to maintain as much symmetry as possible, we transpose the first $N/2$ entries of the last row to the first $N/2$ entries of the $(N+1)$-th column. For the remaining $N/2$ entries of the $(N+1)$-th column, we use the vector $[2n-1\ 1\ 3\ \ldots\ 2n-3]^T$, in order to make every column a permutation. Therefore, only $N/2$ entries in the last row and $N/2$ entries in the last column do not satisfy the requirement that they have complementary and opposite current loops at the distances from the normal group. To overcome that, we construct a right routing matrix to provide those complementary and opposite current loops (see the routing matrix for $N = 8$).

The most direct approach is to generate as the bottom row for the right routing matrix the following pattern:

$$[2n-1\ 1\ 3\ \ldots\ 2n-3\ 2n-1\ 1\ 3\ \ldots\ 2n-3\ 0].$$

This can be achieved easily by taking C_1 in the left routing matrix, and swapping 1 with 2, 3 with 4, and in general $2i-1$ with $2i$. $C_1' = [2\ 1\ 4\ 3\ \ldots\ 2n\ 2n-1]^T$ is the resultant vector. We can apply the same construction as before to obtain the right routing matrix.

Note that the routing matrix is not unique. An alternative routing matrix can be obtained by simply permuting the columns in the original one.

4.2 Caveats

The twisted-bundle structure can significantly eliminate the coupling inductances between signal nets in the twisted group and the normal group if the assumptions that every signal net in a group share a common return path, and there is a return path for each group hold. If these assumptions are not valid, then the structure may fail to eliminate the mutual inductances between two groups, or can only eliminate a portion of the mutual inductance. For the top few signal nets in the normal group, for example, they are equally close to the ground lines above and below them. In this case, current in these signal nets may return through the upper ground line. Nonetheless, for nets in the bottom half of the normal group, they are more likely to use only the lower return path. Again, we assume that quiet or opposite-switching neighboring nets are not ideal return paths because the current would have to go through highly resistive devices.

The mutual inductances between two groups are significantly reduced. It is natural for one to ask the following question: within a group (be it the twisted group or the normal group), is it possible to reduce the mutual inductances for signal nets within one group as we do between two groups? The answer is no. As long as two signal nets share one common return path, the mutual inductance can not be reduced by net reordering. We prove this in the following.

There are four relative positions for two signal lines and the common ground line as illustrated in Figure 5. We examine the inductive noise induced by signal 1 on signal line 2. We assume that the current in signal 1 flows from the left to right, and that it is increasing. The directions of the magnetic flux produced are depicted by the round direction symbols in Figure 5. By the Faraday's law, the inductive noise (emf) on signal 2 will try to counteract the change of magnetic flux in the loop formed by signal 2 and the ground. Therefore, in each of the four cases, the direction of this induced voltage drop on signal 2 is from the right to left, as shown in Figure 5. Hence, the mutual inductance cannot be eliminated.

5. EXPERIMENTAL RESULTS

Based on the twisted-bundle structure, a 16-bit bus is designed, as shown in Figure 6. The 16 signals are divided into four groups, with 4 signals in each group. Twisted groups and normal groups are alternated. To join the adjacent routing regions in the twisted groups, another metal layer is used. Figure 7 shows part of the stick diagram of the twisted group. In a normal group, the ground line is in the middle, sandwiched between two signal lines above it and two below it.

To show the advantage of the twisted-bundle structure, a traditional 16-bit bus, which consists of 4 normal groups, is constructed for comparison. We refer to it as the normal structure. The inductance matrix for the two kinds of buses are shown below. Only the first four columns of the 16x16 matrix are shown. Rows 1 through 4 are for nets within the first group; the rest are the coupling inductance between nets in the first group and the remaining groups. We assume that the buses are $2mm$ long. For all the metal wires, the thickness is $1\mu m$, and the width and spacing are both assumed

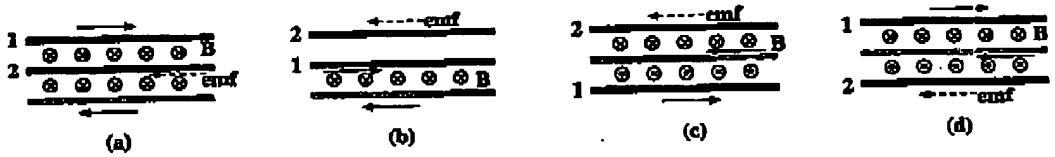

Figure 5: Two signals sharing a common return path.

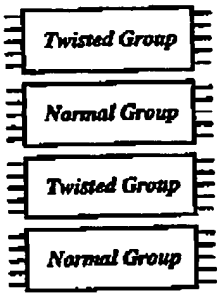

Figure 6: A 16-bit signal bus in a twisted-bundle structure.

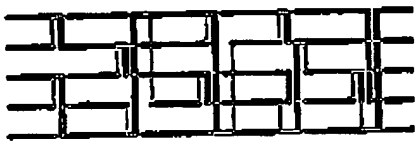

Figure 7: Stick diagram of the layout for a twisted group (not drawn to scale).

to be $1\mu m$. The spacing between the two metal layers is $1\mu m$. The inductance matrix of the twisted-bundle structure is given below:

$$\begin{pmatrix} 1.5e-09 & 5.9e-10 & 8.2e-10 & 8.4e-10 \\ 5.9e-10 & 1.5e-09 & 8.4e-10 & 8.2e-10 \\ 8.2e-10 & 8.4e-10 & 1.8e-09 & 1.1e-09 \\ 8.4e-10 & 8.2e-10 & 1.1e-09 & 1.8e-09 \\ 3.6e-13 & 5.2e-13 & 5.4e-13 & 1.0e-12 \\ 2.6e-13 & 3.2e-13 & 1.7e-13 & 3.6e-13 \\ 2.0e-13 & 2.5e-13 & 1.1e-13 & 2.4e-13 \\ 3.6e-13 & 4.4e-13 & 1.9e-13 & 4.1e-13 \\ 1.2e-11 & 8.1e-13 & 9.8e-12 & 9.8e-12 \\ 7.9e-13 & 1.2e-11 & 9.8e-12 & 9.7e-12 \\ 1.1e-11 & 8.7e-12 & 2.7e-11 & 2.1e-11 \\ 8.8e-12 & 1.1e-11 & 2.1e-11 & 2.7e-11 \\ 7.2e-14 & 9.3e-14 & 4.0e-14 & 8.0e-14 \\ 3.3e-14 & 4.3e-14 & 1.9e-14 & 3.7e-14 \\ 2.9e-14 & 3.8e-14 & 1.6e-14 & 3.3e-14 \\ 5.5e-14 & 7.2e-14 & 3.1e-14 & 6.2e-14 \end{pmatrix}$$

Table 1: Input patterns for investigating the noise levels in signal 8.

Wire Index:	0123456789ABCDEF
Pattern 1	0000000f0f000000
Pattern 2	0000fffr0fff0000
Pattern 3	0000fffr0rfff000
Pattern 4	ffffffff0ffffffff
Pattern 5	ffffffffr0rffffff

The inductance matrix of the normal structure is given below:

$$\begin{pmatrix} 1.8e-09 & 8.8e-10 & 4.4e-10 & 6.0e-10 \\ 8.8e-10 & 1.2e-09 & 3.2e-10 & 4.4e-10 \\ 4.4e-10 & 3.2e-10 & 1.2e-09 & 8.8e-10 \\ 6.0e-10 & 4.4e-10 & 8.8e-10 & 1.8e-09 \\ 7.0e-11 & 4.2e-11 & 7.3e-11 & 2.3e-10 \\ 2.8e-11 & 1.6e-11 & 2.6e-11 & 7.3e-11 \\ 2.0e-11 & 1.1e-11 & 1.6e-11 & 4.2e-11 \\ 3.4e-11 & 2.0e-11 & 2.8e-11 & 7.0e-11 \\ 1.6e-11 & 9.0e-12 & 1.1e-11 & 2.6e-11 \\ 7.3e-12 & 4.0e-12 & 5.0e-12 & 1.1e-11 \\ 6.1e-12 & 3.3e-12 & 4.0e-12 & 9.0e-12 \\ 1.1e-11 & 6.1e-12 & 7.3e-12 & 1.6e-11 \\ 7.2e-12 & 3.8e-12 & 4.4e-12 & 9.6e-12 \\ 3.3e-12 & 1.8e-12 & 2.0e-12 & 4.4e-12 \\ 2.9e-12 & 1.6e-12 & 1.8e-12 & 3.8e-12 \\ 5.6e-12 & 2.9e-12 & 3.3e-12 & 7.2e-12 \end{pmatrix}$$

As we can see, the mutual inductances between signal nets within the first group are similar in both matrices. The mutual inductances between signal nets in the first twisted group and the two normal groups are about two orders of magnitude smaller than those between corresponding nets in the normal structure. The mutual inductances between the two twisted groups are not zero. As the two groups are separated by a normal group, the distance between them makes the mutual inductances smaller than those in the first group.

We also extract the capacitance and inductance values for different wire lengths, and simulate the resulting RLC networks in SPICE using different input patterns at $1GHz$ and $2GHz$ signal frequencies. Wire lengths are $1mm$, $2mm$ and $4mm$, representing typical top-level global wires between repeaters or gates in high-speed circuits [5]. For all traces, the drivers are $160X$ of the minimum inverter in a representative $0.18\mu m$ CMOS technology with $1.5V$ V_{dd}, and the receivers are $40X$ of the minimum inverter.

Table 1 describes the input patterns used in the simulations. We index the signals in a 16-bit bus from 0 to F. Note that wire 0 here is not the ground wire. In this table, 'r', 'f', and '0' stand for 'rising', 'falling', and 'quiet', respectively. The rise and fall times of the signals are assumed to be one-tenth of the clock period. All

Table 2: Comparison of noise levels between the twisted-bundle and normal structures.

Length (*mm*)	Input Pattern	Noise (*V*) freq=1*GHz* Twisted	freq=1*GHz* Normal	freq=2*GHz* Twisted	freq=2*GHz* Normal
1	1	0.05	0.17	0.07	0.25
	2	0.23	0.25	0.32	0.40
	3	0.13	0.16	0.18	0.28
	4	0.23	0.26	0.38	0.39
	5	0.12	0.18	0.18	0.28
2	1	0.09	0.36	0.11	0.42
	2	0.38	0.46	0.44	0.55
	3	0.18	0.35	0.23	0.46
	4	0.37	0.47	0.44	0.55
	5	0.18	0.34	0.23	0.48
4	1	0.14	0.55	0.15	0.59
	2	0.51	0.66	0.53	0.67
	3	0.21	0.51	0.23	0.55
	4	0.53	0.66	0.54	0.68
	5	0.23	0.49	0.24	0.55

Table 3: Comparison of maximum delays between the twisted-bundle and normal structures.

Length,freq	Maximum delay (*ns*) Twisted Structure twisted	Twisted Structure normal	Normal Structure
1*mm*,1*GHz*	0.040	0.041	0.041
1*mm*,2*GHz*	0.033	0.033	0.034
2*mm*,1*GHz*	0.069	0.073	0.072
2*mm*,2*GHz*	0.061	0.067	0.065
4*mm*,1*GHz*	0.140	0.146	0.145
4*mm*,2*GHz*	0.129	0.138	0.137

switching signals switch at the same time. Table 2 shows the noise levels measured at the far end of the victim signal 8. From the simulation results, we observe that the twisted-bundle structure can effectively reduce the coupling noise. For 1*mm* wire, we achieve 4% to 72% noise reduction; for 2*mm* wire, 18% to 76%; and for 4*mm* wire, 20% to 75%. Similar results are obtained when we use input patterns obtained by substituting '1' for '2' and '2' for '1' in the five input patterns listed in Table 1.

The impact of the twisted-bundle structure on signal delay is also investigated. The input patterns are similar to those in Table 1 except that signal 8 is also switching (both high and low) instead of being quiet. Table 3 summarizes the maximum delays found for the twisted-bundle and normal structures. The second and third columns in Table 3 list the maximum delays of nets in the twisted groups and normal groups of the twisted-bundle structure, respectively; the fourth column lists the maximum delays of nets in the normal structure. Although every wire in a twisted group has a longer wire length, a higher resistance, and a higher capacitance than wires in a normal group, the simulation results show that wire twisting has minimal impact on the maximum delays. The maximum delays for twisted wires and normal wires in the twisted-bundle structure do not differ by more than 10%. The differences between the maximum delays of the twisted structure and normal structure are even smaller.

6. CONCLUSION

In this paper, we present the *twisted-bundle* layout structure. Inductance extraction with FastHenry shows the effectiveness of this structure in minimizing mutual inductance. SPICE simulation results also show that it can considerably reduce the coupling noise.

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Docket No.: 42390.P13294

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of:
Lyn Mark Elzinga

Application No. 10/040,536

Filed: December 28, 2001

For: INTERCONNECT SWIZZLING FOR CAPACATIVE AND INDUCTIVE NOISE CANCELLATION

Examiner: Vuthe Siek

Art Unit: 2825

CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the United States Patent and Trademark Office, Fax No. (703) 872-9306 on 6/25/04

Date Lawrence M. Mennemeier

APPELLANT'S BRIEF UNDER 37 CFR § 1.192
IN SUPPORT OF APPELLANT'S APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Mail Stop Appeal Brief-Patents
Commissioner of Patents
PO Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellant hereby submits this Brief in triplicate in support of an appeal from a final decision of the Examiner, in the above-referenced case. Appellant respectfully requests consideration of this appeal by the board of Patent Appeals and Interference for allowance of the above-referenced patent application.

TABLE OF CONTENTS

I. Real Party in Interest

The real party in interest in the present appeal is Intel Corporation of Santa Clara, California, the assignee of the present application.

II. Related Appeals and Interferences

There are no related appeals or interferences to appellant's knowledge that would have a bearing on any decision of the Board of Patent Appeals and Interferences.

III. Status of the Claims

Claims 1-23 and 26-38 are allowed

Claims 24 and 25 stand rejected under 35 USC § 102(b) as allegedly being anticipated by US Patent 5,534,732 (DeBrosse).

IV. Status of Amendments

A preliminary amendment, submitted by appellant on 6/7/2002 was entered. An official response to a first Office Action mailed 7/15/2003 was submitted by appellant on 11/17/2003 and was entered. A Final Office Action was mailed on 1/28/2004. Appellant responded by submitting an amendment and official response after final on 3/23/2004, which was entered and an Advisory Action was mailed 5/4/2004. A Notice of Appeal was transmitted on 4/28/2004, and an appeal ensued.

Accordingly, the claims stand as of the entered amendment of 3/23/2004, and are reproduced in clean form in the Appendix.

V. Summary of the Invention

Appellant's disclosure describes a process to employ swizzling that provides capacitive and inductive noise cancellation on a set of concurrently active signal lines. A positive noise due to a capacitive coupling between an attacker signal line and a near victim signal line is, in part, cancelled by a negative or opposite noise due to an inductive coupling between the attacker signal line and a far victim signal line. A swizzling pattern is set forth whereby signal lines of one segment are reordered to transpose near victim signal lines and far victim signal lines in subsequent segments to facilitate the capacitive and inductive cancellation. The swizzling pattern is selected to further facilitate similar capacitive and inductive noise cancellation among the other signal lines of the set.

In some embodiments, the process continues to employ the swizzling pattern in multiple stages to place each signal line adjacent to every other signal line of the set in some swizzle stage. In some alternative embodiments, swizzling patterns may be selected which place each signal line adjacent to every other signal line of the set in some predetermined number of swizzle stages. Subsequent stages of swizzling provide the set of signal lines with capacitive and inductive noise cancellation in addition to the capacitive and inductive noise cancellations of previous stages. The signal lines are optionally reordered by a final swizzle stage to restore the set's original order. In some embodiments, swizzling patterns may be selected from cyclic swizzle groups such that repeating the swizzling pattern automatically restores the set's original order and/or places each signal line adjacent to other signal lines of the set in a predetermined number of swizzle stages.

In some embodiments, a plurality of S swizzle stages may be inserted to provide capacitive and inductive noise cancellation within a set of N concurrently active signal lines, S being computed for a particular value of N according to the equation:

$$N^2/2 - (2S+3)N/2 + S + 1 = 0.$$

VI. Issues

1. Is claim 24 anticipated by DeBrosse?

2. Is claims 25 anticipated by DeBrosse?

VII. Grouping of Claims (Independent Claims **Bolded**)

For the purposes of this appeal, claims **24** and 25 do not stand or fall together.

Group I: Means for Providing Multiple Capacitive and Inductive Noise Cancellation Stages.

Claim **24**.

Group II: Means for Providing Multiple Capacitive and Inductive Noise Cancellation Stages and Restoring Initial Order.

Claim 25.

VIII. Argument

A. Claim 24 Is Not Anticipated by DeBrosse

Claim 24 stands rejected under 35 USC § 102(b) as allegedly being anticipated by US Patent 5,534,732 (DeBrosse).

The MPEP § 2131 states that:

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Appellant respectfully submits that in the cited reference, each and every element as set forth in the Group I claim is not found, either expressly or inherently described.

Claim 24, for example, sets forth:

24. (Original) An interconnect comprising:
a set of N active signal lines having an initial order;
means for providing the set of signal lines with a first capacitive and inductive noise cancellation; and;
means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation.

The invention of DeBrosse relates to a single crossing region that traverses paired true/complement line conductors such that intra-pair capacitive coupling is avoided and inter-pair capacitive coupling is matched (abstract; col. 2, lines 47-51; Figs 5 and 7-10).

The Final Office Action states (emphasis added):

"DeBrosse et al. teach an interconnection layout comprising a set of N active signal lines having an initial order (as shown in Figure 5 for example); means for providing the set of signal lines with a first capacitive and inductive noise cancellation; and means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation (shown in Figure 5 for example). DeBrosse et al. show capacitive noise cancellation. Since capacitive and inductive parasitics are inherently included in conductive line[s], thus capacitive noise cancellation inherently includes inductive noise cancellation."

Appellant respectfully disagrees. Appellant submits that (1) in the first region of

DeBrosse, the signal lines are in their initial order where DeBrosse states that intra-pair capacitive coupling between true and complement lines is avoided not cancelled (col. 6, lines 1-23; Fig. 5).

Appellant further submits that (2) in the second region of DeBrosse, capacitive coupling between pairs is matched such that a line which was disposed adjacent to a true signal line of a pair in the first region is then disposed adjacent to the complemented signal line of the pair in the second region and vise-versa. For example the signal labeled 2-bar is adjacent to the signals labeled 1-bar and 3 in the first region and then adjacent to their complements labeled 1 and 3-bar in the second region (Fig. 5). Thus, in DeBrosse, the set of signal lines is provided with a single cancellation of the capacitive couplings from the true and complemented signal lines (col. 6, lines 1-27; Fig. 5).

On the other hand, claim 24 sets forth means for providing the set of signal lines with a first capacitive and inductive noise cancellation, and means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation. DeBrosse does not describe, either expressly or inherently, providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation.

Appellant further submits that (3) from the presence of inductive parasitics in line conductors it can not be concluded that capacitive noise cancellation inherently includes inductive noise cancellation.

In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999):

> To establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by

persons of ordinary skill." Continental Can Co. v. Monsanto Co. , 948 F.2d 1264, 1268, 20 U.S.P.Q.2d 1746, 1749 (Fed. Cir. 1991).

The existence of inductive parasitics does not make it clear that the missing descriptive matter, "capacitive and inductive noise cancellation," is necessarily present in the technique described in the reference. The examiner does not provide objective evidence or cogent technical reasoning to support the conclusion of inherency. Capacitive coupling is strongly related to the proximity of the signal lines, which is addressed by DeBrosse. On the other hand, for inductive coupling it is not so much the proximity of a signal line to an attacker signal line as it is the surface area of a current loop or current loops formed by the attacker signal line and its closest return path, which is not addressed by DeBrosse. One signal line may be inductively coupled to many or all of the other signal lines and DeBrosse addresses only adjacent signal lines and their paired complement signal lines.

Appellant provides the following article as extrinsic evidence that the missing descriptive matter would not be recognized by one of skill in the art as being necessarily present in the technique described by DeBrosse.

Exhibit A: Guoan Zhong et al., A Twisted-Bundle Layout Structure for Minimizing Inductive Coupling Noise, *International Conference on Computer-Aided Design*, Nov. 5-9, 2000.

Referring to subsection 4.2 titled "Caveats," paragraphs 2 and 3 and Figure 5, the authors address the question of whether it is possible to reduce mutual inductances within a group of signal lines sharing a common return (such as the one shown in Fig. 11 of DeBrosse) by reordering the positions of signal lines within the group. They conclude that it is not.

Finally, appellant submits that (4) DeBrosse should not be considered equivalent

under 35 U.S.C. 112, paragraph six, to the subject matter set forth in claim 24.

The MPEP § 2181 states that:

> When making a determination of patentability under 35 U.S.C 102 or 103, past practice was to interpret a "means or step plus function" limitation by giving it the "broadest reasonable interpretation." Under the PTO's long-standing practice this meant interpreting such a limitation as reading on any prior art means or step which performed the function specified in the claim without regard for whether the prior art means or step was equivalent to the corresponding structure, material or acts described in the specification. However, in Donaldson, the Federal Circuit stated:
>
> Per our holding, the "broadest reasonable interpretation" that an examiner may give means-plus-function language is that statutorily mandated in paragraph six. Accordingly, the PTO may not disregard the structure disclosed in the specification corresponding to such language when rendering a patentability determination.

While appellant intends that the broadest reasonable interpretation should be given to claims 1-23 and 28-38, all of which have been allowed, the means-plus-function form of claim 24 may not be modified by language containing sufficient structure, material or acts for achieving the specified function. Therefore claim 24 should be construed to cover the corresponding structure, material or acts described in the specification and equivalents thereof.

The MPEP § 2181 also states that:

> [U]nless an element performs the identical function specified in the claim, it cannot be an equivalent for the purposes of 35 U.S.C. 112, sixth paragraph. Pennwalt Corp. v. Durand-Wayland, Inc., 833 F.2d 931, 4 USPQ2d 1737 (Fed. Cir. 1987), cert. denied, 484 U.S. 961 (1988).

For example, as described in paragraph [0041] of the specification for the present application, in a process to employ swizzling that may provide capacitive and inductive noise cancellation on a set of signal lines, a positive noise due to a capacitive coupling between an attacker signal line and a first victim signal line is, in part, cancelled by a negative or opposite noise due to an inductive coupling between the attacker signal line and a second victim signal line.

Paragraph [0046] explains a key observation is that by reversing the positions of

the near victim signal line and far victim signal line with respect to the attacker in a subsequent interconnect segment, a partial cancellation of the capacitive and inductive noise voltages may be provided. Therefore, it will be appreciated that a partial cancellation of capacitive and inductive noise may be provided in a subsequent interconnect segment by a swizzling of a set of signal lines.

Paragraph [0049] also explains that typically the inductive noise from one attacker is weaker than the capacitive noise form one attacker. A key observation is that additional swizzling may be used to provide subsequent stages of further capacitive and inductive noise cancellation for the set by balancing the number of signal lines that are near neighbors in subsequent stages.

DeBrosse does not suggest capacitive and inductive noise cancellation as disclosed in appellant's specification or equivalents thereof, but rather shows a technique for avoidance of capacitive coupling between pairs of true/complement line conductors, and capacitive matching between the true/complement line conductors of one pair and those of its neighbor pairs (col. 1, lines 11-15, col. 2, lines 56-67 and col. 3, lines 1-5). DeBrosse admits that his layout is applicable only to interconnection arrays having a plurality of paired true/complement line conductors (col. 3, lines 28-30).

Appellant respectfully submits that a person of ordinary skill in the art would not have recognized an interchangeability of DeBrosse (which relies upon capacitive matching between the true/complement line conductor pairs) and the capacitive and inductive noise cancellation disclosed in appellant's specification (which does not rely upon such characteristics of true/complement line conductors).

Even if capacitive matching between the true/complement line conductors could

be considered equivalent to the capacitive and inductive noise cancellation function set forth in claim 24, DeBrosse performed it in a substantially different way (by alternating the capacitive coupling of true and complement line conductors and requiring twice as many signal lines as the method disclosed in appellant's specification) with a substantially different result (a single crossing region versus repeatedly swizzling to balance the number of signal lines that are near neighbors for subsequent capacitive and inductive noise cancellation).

DeBrosse does not expressly or inherently describe equivalent means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation. DeBrosse shows a technique including, "forming a single crossing region including crossing the line conductors of each pair once;" (col. 3, lines 13-15). DeBrosse discloses reordering the signal lines only once (col. 3, lines 22-24 and col. 7, lines 63 through col. 8, line 2). Even DeBrosse's title, "Single Twist Layout and Method for Paired Line Conductors of Integrated Circuits," admits the nonequivalence of the prior art element of DeBrosse for allegedly performing the function set forth in claim 24.

Accordingly in light of the argument presented above, appellant respectfully submits that independent claim 24 is not anticipated by DeBrosse.

B. Claim 25 Is Not Anticipated by DeBrosse

Claim 25 stands rejected under 35 USC § 102(b) as allegedly being anticipated by US Patent 5,534,732 (DeBrosse).

In accordance with the arguments presented above with regard to the patentability of claim 24, appellant believes that claim 25 is patentable, first, for including all of the limitations of claim 24, and additionally for the reasons described below.

The MPEP § 2131 states that:

> "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Appellant respectfully submits that in the cited reference, each and every element as set forth in the Group II claim is not found, either expressly or inherently described in as complete detail as is contained in the claim.

Claim 25, for example, sets forth:

> 25. (Original) The interconnect of Claim 24 further comprising:
> means for restoring the initial order of the set of signal lines.

As stated above, the invention of DeBrosse relates to a single crossing region that traverses paired true/complement line conductors such that intra-pair capacitive coupling is avoided and inter-pair capacitive coupling is matched (abstract; col. 2, lines 47-51). Clearly, the initial order of the set of signal lines is not restored by the single crossing region of DeBrosse (see for example Figs 5 and 7-10).

The Final Office Action states:

> "DeBrosse et al. teach that signal lines in the crossing region are reordered in the third region in order to obtain initial signal lines in the first region or as original signal lines configuration in initial stage, where the signal lines are substantially parallel (Please se Figs. 5, 7, 8, 9, 10 and 11)."

Appellant respectfully disagrees. Appellant submits that (1) in the first region of

DeBrosse, the signal lines are in their initial order and that initial order is not restored by any means.

Referring to Figure 5, for example, DeBrosse states that in the first region line conductor 1 is disposed adjacent to line conductor 2 and line conductor 1-bar is disposed adjacent to line conductor 2-bar (col. 6, lines 1-6). In contrast, opposite the crossing region, line conductor 1 is disposed adjacent to line conductor 2-bar and line conductor 2 is disposed adjacent to line conductor 3-bar, which is not the same order as their initial order (col. 6, lines 7-13). DeBrosse refers to the pattern applied to initially ordered lines 1, 2, 1-bar, and 2-bar respectively as "down 1," "down 3," "up 3," and "up 1," (col. 6, lines 16-17).

Further, as stated above with regard to claim 24, the means-plus-function form of claim 25 may not be modified by language containing sufficient structure, material or acts for achieving the specified function. Therefore claim 25 should be construed to cover the corresponding structure, material or acts described in the specification and equivalents thereof.

Appellant submits that (2) DeBrosse should not be considered equivalent under 35 U.S.C. 112, paragraph six, to the subject matter set forth in claim 25.

For example, as described in paragraphs [0094] and [0095] of the specification for the present application with reference to Figure 10, it will be appreciated that repeated compositions of c and d generate swizzle groups with respect to an initial order {1,2,3,4,5,6,7,8} as follows:

$$c^1 = \{7,4,1,3,6,8,5,2\}, \quad d^1 = \{2,4,1,6,3,8,5,7\},$$

$$c^2 = \{5,3,7,1,8,2,6,4\}, \quad d^2 = \{4,6,2,8,1,7,3,5\},$$

$c^3 = \{6,1,5,7,2,4,8,3\}$, $d^3 = \{6,8,4,7,2,5,1,3\}$,

$c^4 = \{8,7,6,5,4,3,2,1\}$, $d^4 = \{8,7,6,5,4,3,2,1\}$,

$c^5 = \{2,5,8,6,3,1,4,7\}$, $d^5 = \{7,5,8,3,6,1,4,2\}$,

$c^6 = \{4,6,2,8,1,7,3,5\}$, $d^6 = \{5,3,7,1,8,2,6,4\}$,

$c^7 = \{3,8,4,2,7,5,1,6\}$, $d^7 = \{3,1,5,2,7,4,8,6\}$,

$c^8 = \{1,2,3,4,5,6,7,8\}$, $d^8 = \{1,2,3,4,5,6,7,8\}$.

It will be further appreciated that a swizzling pattern given by c^1, c^1, c^1, c^5, may be employed using swizzling 1041 repeatedly and optionally restoring the initial order of the set using swizzling 1045.

Similarly, Figures 4a-b, 10a-c, 11b, and 13a-d illustrate alternative embodiments where the initial order of a set of signal lines may be restored by swizzling patterns which may be conveniently selected from swizzle groups.

DeBrosse does not expressly or inherently describe equivalent means for restoring the initial order of the set of signal lines. The techniques of DeBrosse use a single crossing region crossing the line conductors of each pair only once and reordering the signal lines exactly once (col. 3, lines 13-24 and col. 7, lines 63 through col. 8, line 2).

Appellant respectfully submits that a person of ordinary skill in the art would not have recognized an interchangeability of the single crossing region of DeBrosse and the swizzling patterns disclosed in appellant's specification for restoring the initial order of the set of signal lines.

Additionally, appellant believes that since the single crossing region of DeBrosse performs a substantially different function (matching true/complement signal line pairs) in a substantially different way (reordering the signal lines exactly once), it is not

equivalent for allegedly performing the function of restoring the initial order of the set of signal lines set forth in claim 25.

Accordingly in light of the argument presented above, appellant respectfully submits that dependent claim 25 is not anticipated by DeBrosse.

Conclusion

Appellant submits that all claims now pending are in condition for allowance. Such action is earnestly solicited at the earliest possible date. If there is a deficiency in fees, please charge our Deposit Acct. No. 02-2666.

Respectfully submitted,

Date: 6/25/2004

Lawrence M. Mennemeier, Reg. No. 51,003

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IX. Appendix A: Claims Allowed and Involved in Appeal (Clean Copy)

1. (Original) A method comprising:

swizzling a set of N concurrently active signal lines into a first order to provide a first stage of capacitive and inductive noise cancellation for a first plurality of signal lines of the set; and

swizzling the set of N concurrently active signal lines again into a second order different from the first order to provide a second stage of further capacitive and inductive noise cancellation for the first plurality of signal lines of the set.

2. (Original) The method of Claim 1 wherein a first signal line of the set is adjacent to a first subset of the set of N concurrently active signal lines in the first stage and swizzling the set of N concurrently active signal lines again places the first signal line adjacent to a second subset of the set of N concurrently active signal lines in the second stage, the first subset and the second subset being disjoint.

3. (Original) The method of Claim 2 wherein the first signal line of the set is adjacent to a third subset of the set of signal lines in an initial order of the set of N concurrently active signal lines and swizzling the set of signal lines places the first signal line adjacent to the first subset of signal lines in the first stage, the first subset and the third subset being disjoint.

4. (Original) The method of Claim 1 wherein the set of N concurrently active signal lines have a substantially common origin and a substantially common destination.

5. (Original) The method of Claim 1 wherein swizzling the set of N concurrently active signal lines comprises reordering N signal lines for concurrently carrying N bits of information in substantially parallel signal tracks on a substantially planar substrate by

routing each of a second plurality of said N signal lines from a corresponding pre-swizzling signal track directly to a corresponding post-swizzling signal track, optionally via a substantially parallel planar layer.

6. (Original) The method of Claim 5 wherein each swizzling of the set of N concurrently active signal lines is accomplished by inserting a single swizzle cell.

7. (Original) The method of Claim 1 comprising swizzling the set of N concurrently active signal lines to provide S stages of capacitive and inductive noise cancellation and optionally providing an additional stage to restore an initial order of the set, wherein each of the N concurrently active signal lines of the set is placed adjacent to every other signal line of the set in some stage of the S stages, S being computed from N according to the equation:

$$N^2/2 - (2S+3)N/2 + S + 1 = 0.$$

8. (Original) An article of manufacture comprising

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the method of Claim 7.

9. (Original) An article of manufacture comprising

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the method of Claim 6.

10. (Original) An article of manufacture comprising

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the method of Claim 3.

11. (Original) An article of manufacture comprising

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform the method of Claim 1.

12. (Original) The method of Claim 1 wherein the first stage of capacitive and inductive noise cancellation and the second stage of further capacitive and inductive noise cancellation reduce capacitive and inductive noise due to switching within the set of signal lines.

13. (Original) The method of Claim 1 wherein concurrently active indicates that each of the N signal lines may be switched in a single transmission cycle.

14. (Original) An apparatus comprising:

a set of N signal lines configurable to transmit N bits of information in a transmission cycle, the signal lines being substantially parallel and having a first portion with a first signal line order;

a first swizzle stage of the set of N signal lines having a second portion with a second signal line order, wherein a first signal line of the set is adjacent to a first subset of the N signal lines in said first portion and the first signal line is adjacent to a second subset of the N signal lines in said second portion, the first subset and the second subset being disjoint; and

a second swizzle stage of the set of N signal lines having a third portion with a third signal line order, wherein the first signal line of the set is adjacent to a third subset of the N signal lines in said third portion, the first subset the second subset and the third subset being disjoint.

15. (Original) The apparatus of Claim 14 wherein the set of N signal lines have a substantially common origin and a substantially common destination.

16. (Original) The apparatus of Claim 14 comprising

said set of N signal lines in substantially parallel signal tracks on a substantially planar substrate;

each of a first plurality of the N signal lines being routed from a corresponding

signal track in the first portion, according to the first signal line order, directly to a corresponding signal track in the second portion, according to the second signal line order, optionally via one or more substantially parallel planar layers; and

each of a second plurality of the N signal lines being routed from a corresponding signal track in the second portion, according to the second signal line order, directly to a corresponding signal track in the third portion, according to the third signal line order, optionally via the one or more substantially parallel planar layers.

17. (Original) The apparatus of Claim 14 wherein the first swizzle stage of the set of N lines comprises a swizzle cell coupling the first portion with the second portion.

18. (Original) The apparatus of Claim 17 wherein the second swizzle stage of the set of N lines comprises a swizzle cell coupling the second portion with the third portion.

19. (Original) The apparatus of Claim 14 comprising

a plurality of S swizzle stages to provide capacitive and inductive noise cancellation within the set of N signal lines, wherein each of the N signal lines of the set is placed adjacent to every other signal line of the set in some swizzle stage of the S swizzle stages, S being computed for a particular value of N according to the equation, $N^2/2 - (2S+3)N/2 + S + 1 = 0$; and

an optional final stage to restore an initial order for the set of N signal lines.

20. (Original) The apparatus of Claim 14 wherein the third portion of the second swizzle stage places no signal line, of the set of N signal lines, adjacent to one of the same signal lines that they are adjacent to in the second portion of the first swizzle stage.

21. (Original) The apparatus of Claim 20 wherein the second portion of the first swizzle stage places no signal line, of the set of N signal lines, adjacent to one of the same signal lines that they are adjacent to in the first portion.

22. (Original) The apparatus of Claim 21 wherein the third portion of the second swizzle stage places no signal line, of the set of N signal lines, adjacent to one of the same signal lines that they are adjacent to in the first portion.

23. (Original) The apparatus of Claim 14 comprising

a first swizzle cell to reorder the set of N signal lines from the first signal line order into the second signal line order;

a second swizzle cell to reorder the set of N signal lines from the second signal line order into the third signal line order; and

an optional third swizzle cell to restore an initial order for the set of N signal lines.

24. (Original) An interconnect comprising:

a set of N active signal lines having an initial order;

means for providing the set of signal lines with a first capacitive and inductive noise cancellation; and;

means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation.

25. (Original) The interconnect of Claim 24 further comprising:

means for restoring the initial order of the set of signal lines.

26. (Previously Amended) An interconnect comprising:

a set of N active signal lines having an initial order;

means for providing the set of signal lines with a first capacitive and inductive noise cancellation;

means for providing the set of signal lines with a second capacitive and inductive noise cancellation in addition to the first capacitive and inductive noise cancellation; and

means for restoring the initial order of the set of signal lines, wherein the means for restoring the initial order of the set of signal lines provides the set of signal lines with a third capacitive and inductive noise cancellation in addition to the first and second

capacitive and inductive noise cancellations.

27. (Original) The interconnect of Claim 26 wherein the set of signal lines contains an even number of signal lines.

28. (Original) An article of manufacture comprising:

a machine-accessible medium including data that, when accessed by a machine, cause the machine to:

insert a first swizzle stage to provide a set of N concurrently active signal lines having a first signal line order, with a second signal line order, where in the first signal line order, a first signal line of the set is adjacent to a first subset of the N signal lines and in the second signal line order the first signal line is adjacent to a second subset of the N signal lines, the first subset and the second subset having no signal lines in common; and

insert a second swizzle stage to provide the set of N concurrently switched signal lines with a third signal line order, where in the third signal line order the first signal line is adjacent to a third subset of the N signal lines, the first subset, the second subset and the third subset having no signal lines in common.

29. (Original) The article of manufacture of Claim 28 wherein the second signal line order of the first swizzle stage provides a capacitive and inductive noise cancellation by placing the first signal line adjacent to the second subset of the N signal lines.

30. (Original) The article of manufacture of Claim 29 wherein the third signal line order of the second swizzle stage provides an additional capacitive and inductive noise cancellation by placing the first signal line adjacent to the third subset of the N signal lines.

31. (Original) The article of manufacture of Claim 30 wherein the first capacitive and inductive noise cancellation and the additional capacitive and inductive noise cancellation reduce capacitive and inductive noise due to switching within the set of N concurrently

active signal lines.

32. (Original) The article of manufacture of Claim 28 wherein the third signal line order of the second swizzle stage places no signal line, of the set of N concurrently active signal lines, adjacent to one of the same signal lines that they are adjacent to in the second signal line order of the first swizzle stage.

33. (Original) The article of manufacture of Claim 32 wherein second signal line order of the first swizzle stage places no signal line, of the set of N concurrently active signal lines, adjacent to one of the same signal lines that they are adjacent to in the first signal line order.

34. (Original) The article of manufacture of Claim 33 further including data that when accessed by the machine, cause the machine to:

insert a third swizzle stage to restore the set of N concurrently active signal lines to their original order.

35. (Original) The article of manufacture of Claim 28 wherein concurrently active indicates that each of the N signal lines may be switched in a transmission cycle.

36. (Original) The article of manufacture of Claim 28 further including data that when accessed by the machine, cause the machine to:

insert a plurality of S swizzle stages to provide capacitive and inductive noise cancellation within the set of N concurrently active signal lines, wherein each of the N signal lines of the set is placed adjacent to every other signal line of the set in some swizzle stage of the S swizzle stages, S being computed for a particular value of N according to the equation

$$N^2/2 - (2S+3)N/2 + S + 1 = 0;$$ and

insert an optional swizzle to restore an initial order for the set of N concurrently active signal lines.

37. (Original) An apparatus comprising:

a set of N concurrently active signal lines, the signal lines being substantially parallel and having a first signal line order;

a plurality of swizzle cells linking segments of the set of N concurrently active signal lines, the plurality of swizzle cells transposing near victim signal lines and far victim signal lines in subsequent segments to facilitate capacitive and inductive noise cancellation within the set of N concurrently active signal lines; and

an optional swizzle cell to restore an initial order for the set of N concurrently active signal lines.

38. (Original) The apparatus of Claim 37 wherein concurrently active indicates that each of the N signal lines may be switched in a single transmission cycle.

Exhibit A

Guoan Zhong et al., A Twisted-Bundle Layout Structure for Minimizing Inductive Coupling Noise, *International Conference on Computer-Aided Design*, Nov. 5-9, 2000.

A Twisted-Bundle Layout Structure for Minimizing Inductive Coupling Noise*

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ABSTRACT

In this paper, we propose a novel *twisted-bundle* layout structure for minimizing inductive coupling noise. In this structure, we create several routing regions and re-order the routing of nets in each of these routing regions. The purpose is to create complementary and opposite current loops in the twisted-bundle layout structure, such that the magnetic fluxes arising from any signal net within a *twisted group* cancel each other in the current loop of a net of interest. The effectiveness of the twisted-bundle structure in minimizing coupling inductance has been verified by the application of FastHenry extraction on a 16-bit bus structure. We achieve about two orders of magnitude reduction in inductive coupling. SPICE simulations also show that the 16-bit twisted-bundle bus structure is able to maintain high signal integrity at high frequency of operation.

1. INTRODUCTION

Continued scaling of semiconductor technology has brought the issues of interconnect-limited designs to the forefront. The International Technology Roadmap for Semiconductor (ITRS) [1] forecasts that as the VLSI technology advances towards giga-Hertz on-chip frequency and system-level integration on larger die size, self- and coupling-inductances are becoming dominant factors in determining signal delay and signal integrity.

Ref. [16] gave an extensive survey of various noise sources in circuit design. Predominantly, existing studies focused on cross-talk noise due to capacitive coupling. Due to the short range effect of capacitive coupling, techniques such as shielding, net ordering or track permutation have proved to be effective in minimizing capacitive cross-talk noise [6; 17].

On the other hand, inductive effects have a long range effect because they arise from the electromagnetic phenomenon of magnetic flux linking current loops. As a result, inductive noise has a much wider spatial effect than that of a capacitive noise. For this reason, it makes the worst case situation in a circuit much harder to predict. Many of the existing studies that dealt with on-chip inductive effects focused primarily on the modeling and extraction of on-chip interconnect inductance. In [15], loop inductance was calculated in terms of partial inductances defined for wire segments. The Partial Element Equivalent Circuit (PEEC) model was widely used to analyze on-chip inductance [7; 14; 4]. In [9], frequency dependent inductance and resistance were computed based on the magnetoquasistatic assumption, and in [10], a simple layout rule-based method was used to speed up the computation.

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A few recent studies have reported success in minimizing the undesirable inductive effects. In recent Alpha chip designs [2], on-chip inductance was limited by sandwiching lines with high current density between isolating metal planes. In [11], the wiring overhead was reduced by using a interdigitated layout structure, in which a wide wire was split into many lines, interspersed with ground lines. These techniques, however, considered only self-inductance. In [8], inductive coupling noise was reduced by shield insertion and net ordering.

In this paper, we propose a novel *twisted-bundle* layout structure for minimizing inductive coupling noise. By creating complementary and opposite current loops in the layout structure, we achieve two orders of magnitude reduction in inductive coupling. The abilities of the twisted-bundle structure in minimizing coupling inductance and maintaining high signal integrity have been verified by the applications of FastHenry extraction and SPICE simulations on a 16-bit bus structure.

The rest of the paper is organized as follows. In Section 2, preliminaries regarding inductive coupling are explained. In Section 3, we introduce a twisted-pair layout structure, upon which the twisted-bundle structure is based. In Section 4, we present the novel twisted-bundle structure and a systematic approach for synthesizing such a structure. In Section 5, we apply this structure to a 16-bit bus design and compare it with the "traditional" design based on the parasitic parameters extracted by FastHenry and the simulation results by SPICE. Finally, we conclude in Section 6.

2. PRELIMINARIES

Mutual inductances, as well as self inductance, are electromagnetic phenomena that arises from current loops [12; 13]. The inductances for a system of N loops are defined as:

$$L_{ij} = \frac{\Psi_{ij}}{I_j}, \tag{1}$$

where Ψ_{ij} is the magnetic flux in loop i due to a current I_j in loop j. L_{ii} represents the self inductance of loop i, whereas $L_{ij}(i \neq j)$ represents the mutual inductance between loops i and j.

According to the Faraday's law, the mutual inductance can be calculated by finding the magnetic flux linking one loop related to per unit of current in the other loop:

$$M = L_{ij} = \iint_{S_i} \vec{B} \cdot d\vec{S}_i \,/\, I_j, \tag{2}$$

where B is the density of the magnetic flux arising from current I_j in loop i and the integration is over the surface of loop i.

On-chip signal nets form loops with their current return paths; these loops determine the inductances as shown in Eqns. (1) and (2). Therefore, in order to accurately calculate the inductances of

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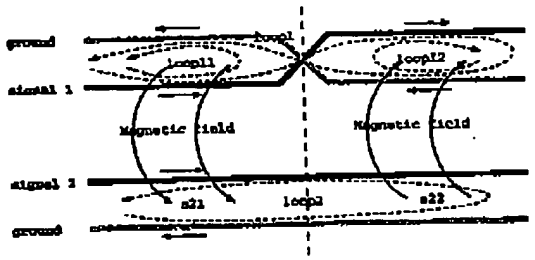

Figure 1: Twisted-pair structure.

on-chip interconnections, it is of critical importance to determine the current return paths of on-chip signal nets. However, it is extremely difficult to find accurate return paths for signal nets, because in the complex interconnection structures that we deal with today, there are several paths through which a current returns [3].

In this work, we assume that all signals use the nearest power/ground line as their return paths [5]. Although quiet or opposite-switching neighboring nets may also serve as return paths, they are not ideal because currents returning from signal wires have to go through devices, which typically have a resistance of several hundred Ohms.

3. TWISTED-PAIR LAYOUT STRUCTURE

From the Faraday's law, there are two possible ways of eliminating the coupling inductance: (i) by creating a magnetic flux that is of an opposite direction; (ii) by eliminating or minimizing the surface area of the second loop. To achieve that, we propose a simple *twisted-pair* layout structure (Figure 1) that is inspired by the twisted-pair wire structure.

As shown in Figure 1, we consider two signal lines in this structure. For each signal line, we assume that there exists a ground line nearby, serving as the signal's dedicated return path. The signal and ground lines are drawn with different shades of gray. Like the twisted-pair wire structure, we intertwine one signal line and its return path at their mid-points such that they are "symmetric" about the mid-points. As the signal and ground lines co-exist on the same metal layer, the physical layout of such a twisted-pair structure involves vias and doglegs.

As indicated in Figure 1, signal lines 1 and 2 form respectively loops $loop_1$ and $loop_2$ with their dedicated return paths. As signal 1 and its return path are twisted, $loop_1$ is divided into two smaller loops: $loop_{11}$ and $loop_{12}$. In quasi-static condition, the current is continuous everywhere along a signal line. Therefore, the two current loops flow in opposite directions, and the magnetic fields caused by $loop_{11}$ and $loop_{12}$ are equal in magnitude, but in opposite directions. According to the Faraday's law in Eqn. (2), the mutual inductance $M = L_{21}$ can be calculated by finding the magnetic flux linking $loop_1$ to $loop_2$:

$$M = \int\int_{s_2} \vec{B} \cdot d\vec{S}_2 \; / \; I_1. \qquad (3)$$

As the integration is over the surface of $loop_2$, we divide the surface of loop into two equal parts S_{21} and S_{22} along the mid-line drawn in Figure 1. We rewrite Eqn. (3) as:

$$M = (\int\int_{s_{21}} \vec{B} \cdot d\vec{S}_{21} + \int\int_{s_{22}} \vec{B} \cdot d\vec{S}_{22}) \; / \; I_1. \qquad (4)$$

When the lengths of the wires are much larger than the spacing between the wires, the magnetic flux linkage in S_{21} mainly comes from $loop_{11}$, and the magnetic flux linkage in S_{22} is primarily due to $loop_{12}$. As the current directions in $loop_{11}$ and $loop_{12}$ are opposite, the directions of the magnetic fluxes in S_{21} and S_{22} are opposite. Therefore, the two integrations over S_{21} and S_{22} cancel each other:

$$\int\int_{s_{22}} \vec{B} \cdot d\vec{S}_{22} = - \int\int_{s_{21}} \vec{B} \cdot d\vec{S}_{21}; \qquad (5)$$

Hence, the mutual inductance between signals 1 and 2 is zero:

$$M = (\int\int_{s_{22}} \vec{B} \cdot d\vec{S}_{21} - \int\int_{s_{21}} \vec{B} \cdot d\vec{S}_{21}) \; / \; I_1 = 0. \qquad (6)$$

In fact, $loop_{12}$ also contributes to the magnetic flux linkage in S_{21}. So does $loop_{11}$ to S_{22}. However, their contributions are quite insignificant, as these two components of magnetic flux also cancel each other in the integration. We can similarly argue that L_{12} is zero because the surfaces of the two loops $loop_{11}$ and $loop_{12}$ actually "sum" to zero.

All the preceding discussions are based on the assumption that the current in a signal line is continuous everywhere. However, this assumption is not valid when the wire length is sufficiently long for the transmission line effect to kick in. If parallel termination is adopted at the receiving ends of signal lines, there are no or minimal reflections at the receiving ends. Consequently, noises gathered at the victim nets cancel each other when they reach the receiving ends. Hence, the mutual inductance is still zero.

We use FastHenry [9] to verify the effectiveness of the proposed twisted-pair layout structure in minimizing coupling inductance. The wire width, height, length, and spacing are $1\mu m$, $2\mu m$, $200\mu m$, and $1\mu m$, respectively.

We extract the inductance matrix under two frequencies: a *high* frequency of $f_H = 10^{16} Hz$ and a *low* frequency of $f_L = 10^6 Hz$. The inductance matrices for a *normal* or *un-twisted* structure are given below:

$$f_H = 10^{16} Hz \quad \begin{pmatrix} 7.4e-11 & 6.2e-12 \\ 6.2e-12 & 7.4e-11 \end{pmatrix} \qquad f_L = 10^6 Hz \quad \begin{pmatrix} 9.1e-11 & 1.0e-11 \\ 1.0e-11 & 9.1e-11 \end{pmatrix}.$$

The diagonal elements are the self-inductances, and off-diagonal entries in the matrix are mutual inductances. The inductance matrices for a *twisted-pair* structure are given below:

$$f_H = 10^{16} Hz \quad \begin{pmatrix} 7.3e-11 & 7.6e-17 \\ 7.8e-17 & 7.4e-11 \end{pmatrix} \qquad f_L = 10^6 Hz \quad \begin{pmatrix} 8.9e-11 & 1.0e-16 \\ 1.1e-16 & 9.1e-11 \end{pmatrix}.$$

The mutual inductances for the twisted-pair structure are about 5 orders of magnitude smaller than the corresponding mutual inductances of the normal un-twisted structure. For all practical purposes, the mutual inductance between signals 1 and 2 is negligible. We also observe that the matrix is not symmetric, i.e, there is a slight discrepancy between L_{12} and L_{21}. The difference may have arisen from numerical errors.

4. TWISTED-BUNDLE STRUCTURE

In this section, we generalize the simple twisted-pair structure such that we can minimize the coupling inductances within a multiple-signal bus that has more than two signal lines. As in the twisted-pair structure, we want to create for each current loop, a complementary and opposite current loop such that the resultant magnetic flux linkage in the current loop of a net of interest is zero.

Figure 2 shows a multiple-bit bus with six signal lines and two ground lines. Here, we assume that the top three signal lines of the 6-bit bus share the ground line labeled 0 as their current return

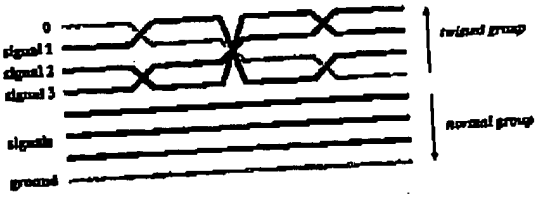

Figure 2: Multiple-signal bus in a twisted-bundle structure.

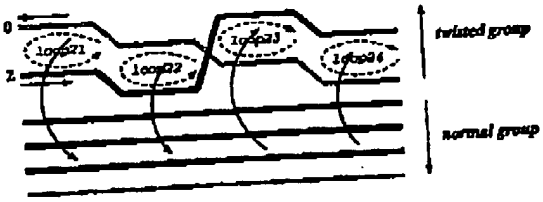

Figure 3: Current loops due to signal line 2 and ground line 0.

paths. The bottom three signal lines share the bottom ground line as their return paths. In the twisted-pair structure, the top signal line and the top ground line are twisted to produce the complementary and opposite current loops. In Figure 2, we twist a *bundle* of the top three signal lines 1, 2, and 3 with the ground line 0, while keeping the bottom three signal lines normal or un-twisted. Hence, we call such a layout structure a *twisted-bundle*, and refer to the group of nets (signal lines and the ground line) that are twisted the *twisted group*. The other group of nets that are not twisted is called the *normal group*.

In the twisted-bundle structure shown in Figure 2, there are four routing regions of equal length in the twisted group. Every signal net in the twisted group goes through the four regions and forms four different loops with the ground line 0. In order to eliminate the mutual inductance, two of the four current loops must form a pair of complementary but opposite loops that are of the same size and of the same distance to the normal group. So do the remaining two current loops. To generate pairs of complementary but opposite loops such that each pair is of the same distance to the normal group, we have to re-order the nets in different routing regions.

Figure 3 illustrates the loops formed by signal 2 and the return path in the four regions. In this example, $loop_{21}$ and $loop_{23}$ cancel each other in the flux linkage of any loop in the normal group, because they are complementary and opposite current loops of the same size, and of the same distance from any loop in the normal group. So do $loop_{22}$ and $loop_{24}$. Hence, the total flux linkage caused by signal 2 (and its return path 0) to any loop in the normal group is equal to zero. Therefore, the mutual inductance between signal 2 and any signal line in the normal group is zero. We can draw similar conclusions for signals 1 and 3.

4.1 Synthesis of Twisted-Bundle

The basic idea of the twisted-bundle structure is to eliminate the mutual inductances, through intelligent net reordering in different routing regions such that the magnetic flux linkages related to one signal-ground pair in different regions cancel each other in the current loop of a net of interest. As the number of the nets in the normal group does not affect the results, the key issue here is the synthesis of the routing pattern in a twisted group.

The order in which the signal nets appear in the twisted bundle defines a *routing matrix*. In a routing matrix, a column represents a routing region in which the net order remains unchanged. For example, the twisted group in Figure 2 corresponds to the following routing matrix:

$$\begin{pmatrix} 0 & 1 & 2 & 3 \\ 1 & 0 & 3 & 2 \\ 2 & 3 & 0 & 1 \\ 3 & 2 & 1 & 0 \end{pmatrix}.$$

In the remainder of this section, we assume that the ground line is labeled 0. We further assume that there are N signal nets labeled 1 through N in the twisted group to be routed. Before we present a systematic approach for synthesizing the routing matrix, we state two observations. First, for the signal nets to be completely routable, each column should be a permutation. Second, in order to generate complementary and opposite current loops, for every signal-ground pair at column x with the signal net, say i, at row y and the ground line 0 at row z, there must exist a column in the matrix such that i is at row z, and 0 at row y. The second observation has two implications:

- There must be at least $(N+1)$ columns in the routing matrix.
- The ground net 0 must appear in all rows in the routing matrix.

We shall now consider the synthesis of a twisted-bundle structure with a odd number of signal nets (i.e., N is odd) and a shared, common ground line. We shall use $N = 7$ to illustrate the idea before presenting the construction of the routing matrix for $N = 2n-1$. A twisted-bundle routing matrix for $N = 7$ is given below:

$$\begin{pmatrix} 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 \\ 1 & 0 & 3 & 4 & 5 & 6 & 7 & 2 \\ 2 & 3 & 0 & 5 & 6 & 7 & 1 & 4 \\ 3 & 4 & 5 & 0 & 7 & 1 & 2 & 6 \\ 4 & 5 & 6 & 7 & 0 & 2 & 3 & 1 \\ 5 & 6 & 7 & 1 & 2 & 0 & 4 & 3 \\ 6 & 7 & 1 & 2 & 3 & 4 & 0 & 5 \\ 7 & 2 & 4 & 6 & 1 & 3 & 5 & 0 \end{pmatrix}$$

For simplicity, we construct the matrix such that the diagonal entries are 0. As a result, the second observation that we stated earlier implies that we should construct a symmetric routing matrix with $(7+1) = 8$ columns if at all possible. To fill in the remaining entries of the matrix, we perform the following tasks:

1. Fill in the first column with $C_1 = [7\,1\,2\,3\,4\,5\,6]^T$ except for the first entry, which is already filled with 0. Displace 7 to the last entry in the column.
2. Perform on $C_1 = [7\,1\,2\,3\,4\,5\,6]^T$ a cyclic shift-up-by-one to obtain $C_2 = [1\,2\,3\,4\,5\,6\,7]^T$.
3. Fill in the second column with C_2 except for the second entry, which is already filled with 0. Displace 2 to the last entry in the column.

In general, we perform on C_i a cyclic shift-up-by-one to obtain C_{i+1}; fill in column $i+1$; and displace the $(i+1)$-th entry in C_{i+1} to the last entry in column $i+1$. We iterate that process until we reach the 8-th column. By symmetry, we can simply transpose the 8-th row to form the routing matrix given above. Following such a construction, we can synthesize the routing matrix for any odd number ($N = 2n-1$) of nets (see Figure 4).

Can we apply such construction rules for even number ($N = 2n$) of signal nets? Observe that in the last row of the routing matrix,

$$\begin{pmatrix}
0 & 1 & 2 & 3 & 4 & \cdots & \cdots & 2n-3 & 2n-2 & 2n-1 \\
1 & 0 & 3 & 4 & \cdots & \cdots & 2n-3 & 2n-2 & 2n-1 & 2 \\
2 & 3 & 0 & \cdots & \cdots & 2n-3 & 2n-2 & 2n-1 & 1 & 4 \\
3 & 4 & \cdots & \cdots & 2n-3 & 2n-2 & 2n-1 & 1 & 2 & \cdots \\
4 & \cdots & \cdots & 2n-3 & 0 & 2n-1 & 1 & 2 & 3 & 2n-2 \\
\cdots & \cdots & 2n-3 & 2n-2 & 2n-1 & 0 & 2 & 3 & 4 & 1 \\
\cdots & 2n-3 & 2n-2 & 2n-1 & 1 & 2 & 0 & 4 & \cdots & 3 \\
2n-3 & 2n-2 & 2n-1 & 1 & 2 & 3 & 4 & \cdots & \cdots & \cdots \\
2n-2 & 2n-1 & 1 & 2 & 3 & 4 & \cdots & \cdots & 0 & 2n-3 \\
2n-1 & 2 & 4 & \cdots & 2n-2 & 1 & 3 & \cdots & 2n-3 & 0
\end{pmatrix}$$

Figure 4: Routing matrix for $N = 2n-1$ signal nets and a common ground line in a twisted group.

the net number in column i is always larger than the net number in column $(i-1)$ by 2 (modulo N). That is because we perform a cyclic shift-up-by-one operation for the vector C_{i-1} and a shift down-by-one for the ground line 0. When $N = 2n-1$, the last row actually forms a permutation. Therefore, we can fill in the last column easily.

When $N = 2n$, however, the last row does not form a permutation. The first eight columns of the following routing matrix are obtained for $N = 8$ signal nets by applying the construction rules outlined earlier:

$$\begin{pmatrix}
0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 & 8 & 0 & 2 & 1 & 4 & 3 & 6 & 5 & 8 & 7 \\
1 & 0 & 3 & 4 & 5 & 6 & 7 & 8 & 2 & 2 & 0 & 4 & 3 & 6 & 5 & 8 & 7 & 1 \\
2 & 3 & 0 & 5 & 6 & 7 & 8 & 1 & 4 & 1 & 4 & 0 & 6 & 5 & 8 & 7 & 2 & 3 \\
3 & 4 & 5 & 0 & 7 & 8 & 1 & 2 & 6 & 4 & 3 & 6 & 0 & 8 & 7 & 2 & 1 & 5 \\
4 & 5 & 6 & 7 & 0 & 1 & 2 & 3 & 7 & 3 & 6 & 5 & 8 & 0 & 2 & 1 & 4 & 8 \\
5 & 6 & 7 & 8 & 1 & 0 & 3 & 4 & 1 & 6 & 5 & 8 & 7 & 2 & 0 & 4 & 3 & 2 \\
6 & 7 & 8 & 1 & 2 & 3 & 0 & 5 & 3 & 5 & 8 & 7 & 2 & 1 & 4 & 0 & 6 & 4 \\
7 & 8 & 1 & 2 & 3 & 4 & 5 & 0 & 5 & 8 & 7 & 2 & 1 & 4 & 3 & 6 & 0 & 6 \\
8 & 2 & 4 & 6 & 8 & 2 & 4 & 6 & 0 & 7 & 1 & 3 & 5 & 7 & 1 & 3 & 5 & 0
\end{pmatrix}$$

It is easy to deduce that in the left half of the preceding matrix, every even-numbered signal net appear twice in the last row as follows:

$$[2n\ 2\ 4\ \ldots\ 2n-2\ 2n\ 2\ 4\ \ldots\ 2n-2\ 0].$$

In order to maintain as much symmetry as possible, we transpose the first $N/2$ entries of the last row to the first $N/2$ entries of the $(N+1)$-th column. For the remaining $N/2$ entries of the $(N+1)$-th column, we use the vector $[2n-1\ 1\ 3\ \ldots\ 2n-3]^T$, in order to make every column a permutation. Therefore, only $N/2$ entries in the last row and $N/2$ entries in the last column do not satisfy the requirement that they have complementary and opposite current loops at the distances from the normal group. To overcome that, we construct a right routing matrix to provide those complementary and opposite current loops (see the routing matrix for $N = 8$).

The most direct approach is to generate as the bottom row for the right routing matrix the following pattern:

$$[2n-1\ 1\ 3\ \ldots\ 2n-3\ 2n-1\ 1\ 3\ \ldots\ 2n-3\ 0].$$

This can be achieved easily by taking C_1 in the left routing matrix, and swapping 1 with 2, 3 with 4, and in general $2i-1$ with $2i$. $C_1' = [2\ 1\ 4\ 3\ \ldots\ 2n\ 2n-1]^T$ is the resultant vector. We can apply the same construction as before to obtain the right routing matrix.

Note that the routing matrix is not unique. An alternative routing matrix can be obtained by simply permuting the columns in the original one.

4.2 Caveats

The twisted-bundle structure can significantly eliminate the coupling inductances between signal nets in the twisted group and the normal group if the assumptions that every signal net in a group share a common return path, and there is a return path for each group hold. If these assumptions are not valid, then the structure may fail to eliminate the mutual inductances between two groups, or can only eliminate a portion of the mutual inductance. For the top few signal nets in the normal group, for example, they are equally close to the ground lines above and below them. In this case, current in these signal nets may return through the upper ground line. Nonetheless, for nets in the bottom half of the normal group, they are more likely to use only the lower return path. Again, we assume that quiet or opposite-switching neighboring nets are not ideal return paths because the current would have to go through highly resistive devices.

The mutual inductances between two groups are significantly reduced. It is natural for one to ask the following question: within a group (be it the twisted group or the normal group), is it possible to reduce the mutual inductances for signal nets within one group as we do between two groups? The answer is no. As long as two signal nets share one common return path, the mutual inductance can not be reduced by net reordering. We prove this in the following.

There are four relative positions for two signal lines and the common ground line as illustrated in Figure 5. We examine the inductive noise induced by signal 1 on signal line 2. We assume that the current in signal 1 flows from the left to right, and that it is increasing. The directions of the magnetic flux produced are depicted by the round direction symbols in Figure 5. By the Faraday's law, the inductive noise (emf) on signal 2 will try to counteract the change of magnetic flux in the loop formed by signal 2 and the ground. Therefore, in each of the four cases, the direction of this induced voltage drop on signal 2 is from the right to left, as shown in Figure 5. Hence, the mutual inductance cannot be eliminated.

5. EXPERIMENTAL RESULTS

Based on the twisted-bundle structure, a 16-bit bus is designed, as shown in Figure 6. The 16 signals are divided into four groups, with 4 signals in each group. Twisted groups and normal groups are alternated. To join the adjacent routing regions in the twisted groups, another metal layer is used. Figure 7 shows part of the stick diagram of the twisted group. In a normal group, the ground line is in the middle, sandwiched between two signal lines above it and two below it.

To show the advantage of the twisted-bundle structure, a traditional 16-bit bus, which consists of 4 normal groups, is constructed for comparison. We refer to it as the normal structure. The inductance matrix for the two kinds of buses are shown below. Only the first four columns of the 16x16 matrix are shown. Rows 1 through 4 are for nets within the first group; the rest are the coupling inductance between nets in the first group and the remaining groups. We assume that the buses are $2mm$ long. For all the metal wires, the thickness is $1\mu m$, and the width and spacing are both assumed

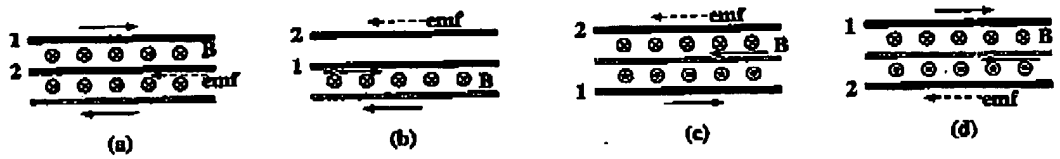

Figure 5: Two signals sharing a common return path.

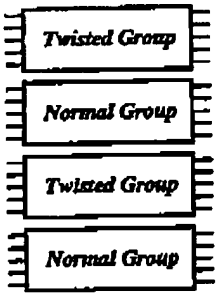

Figure 6: A 16-bit signal bus in a twisted-bundle structure.

Figure 7: Stick diagram of the layout for a twisted group (not drawn to scale).

to be $1\mu m$. The spacing between the two metal layers is $1\mu m$. The inductance matrix of the twisted-bundle structure is given below:

$$\begin{pmatrix} 1.5e-09 & 5.9e-10 & 8.2e-10 & 8.4e-10 \\ 5.9e-10 & 1.5e-09 & 8.4e-10 & 8.2e-10 \\ 8.2e-10 & 8.4e-10 & 1.8e-09 & 1.1e-09 \\ 8.4e-10 & 8.2e-10 & 1.1e-09 & 1.8e-09 \\ 3.6e-13 & 5.2e-13 & 5.4e-13 & 1.0e-12 \\ 2.6e-13 & 3.2e-13 & 1.7e-13 & 3.6e-13 \\ 2.0e-13 & 2.5e-13 & 1.1e-13 & 2.4e-13 \\ 3.6e-13 & 4.4e-13 & 1.9e-13 & 4.1e-13 \\ 1.2e-11 & 8.1e-13 & 9.8e-12 & 9.8e-12 \\ 7.9e-13 & 1.2e-11 & 9.8e-12 & 9.7e-12 \\ 1.1e-11 & 8.7e-12 & 2.7e-11 & 2.1e-11 \\ 8.8e-12 & 1.1e-11 & 2.1e-11 & 2.7e-11 \\ 7.2e-14 & 9.3e-14 & 4.0e-14 & 8.0e-14 \\ 3.3e-14 & 4.3e-14 & 1.9e-14 & 3.7e-14 \\ 2.9e-14 & 3.8e-14 & 1.6e-14 & 3.3e-14 \\ 5.5e-14 & 7.2e-14 & 3.1e-14 & 6.2e-14 \end{pmatrix}$$

Table 1: Input patterns for investigating the noise levels in signal 8.

Wire Index:	0123456789ABCDEF
Pattern 1	0000000f0f000000
Pattern 2	0000ffff0ffff000
Pattern 3	0000ffffr0ffff000
Pattern 4	ffffffff0ffffffff
Pattern 5	ffffffffr0ffffffff

The inductance matrix of the normal structure is given below:

$$\begin{pmatrix} 1.8e-09 & 8.8e-10 & 4.4e-10 & 6.0e-10 \\ 8.8e-10 & 1.2e-09 & 3.2e-10 & 4.4e-10 \\ 4.4e-10 & 3.2e-10 & 1.2e-09 & 8.8e-10 \\ 6.0e-10 & 4.4e-10 & 8.8e-10 & 1.8e-09 \\ 7.0e-11 & 4.2e-11 & 7.3e-11 & 2.3e-10 \\ 2.8e-11 & 1.6e-11 & 2.6e-11 & 7.3e-11 \\ 2.0e-11 & 1.1e-11 & 1.6e-11 & 4.2e-11 \\ 3.4e-11 & 2.0e-11 & 2.8e-11 & 7.0e-11 \\ 1.6e-11 & 9.0e-12 & 1.1e-11 & 2.6e-11 \\ 7.3e-12 & 4.0e-12 & 5.0e-12 & 1.1e-11 \\ 6.1e-12 & 3.3e-12 & 4.0e-12 & 9.0e-12 \\ 1.1e-11 & 6.1e-12 & 7.3e-12 & 1.6e-11 \\ 7.2e-12 & 3.8e-12 & 4.4e-12 & 9.6e-12 \\ 3.3e-12 & 1.8e-12 & 2.0e-12 & 4.4e-12 \\ 2.9e-12 & 1.6e-12 & 1.8e-12 & 3.8e-12 \\ 5.6e-12 & 2.9e-12 & 3.3e-12 & 7.2e-12 \end{pmatrix}$$

As we can see, the mutual inductances between signal nets within the first group are similar in both matrices. The mutual inductances between signal nets in the first twisted group and the two normal groups are about two orders of magnitude smaller than those between corresponding nets in the normal structure. The mutual inductances between the two twisted groups are not zero. As the two groups are separated by a normal group, the distance between them makes the mutual inductances smaller than those in the first group.

We also extract the capacitance and inductance values for different wire lengths, and simulate the resulting RLC networks in SPICE using different input patterns at $1GHz$ and $2GHz$ signal frequencies. Wire lengths are $1mm$, $2mm$ and $4mm$, representing typical top-level global wires between repeaters or gates in high-speed circuits [5]. For all traces, the drivers are 160X of the minimum inverter in a representative $0.18\mu m$ CMOS technology with $1.5V$ V_{dd}, and the receivers are 40X of the minimum inverter.

Table 1 describes the input patterns used in the simulations. We index the signals in a 16-bit bus from 0 to F. Note that wire 0 here is not the ground wire. In this table, 'r', 'f', and '0' stand for 'rising', 'falling', and 'quiet', respectively. The rise and fall times of the signals are assumed to be one-tenth of the clock period. All

Table 2: Comparison of noise levels between the twisted-bundle and normal structures.

Length (*mm*)	Input Pattern	Noise (V) freq=1*GHz* Twisted	freq=1*GHz* Normal	freq=2*GHz* Twisted	freq=2*GHz* Normal
1	1	0.05	0.17	0.07	0.25
	2	0.23	0.25	0.32	0.40
	3	0.13	0.16	0.18	0.28
	4	0.23	0.26	0.38	0.39
	5	0.12	0.18	0.18	0.28
2	1	0.09	0.36	0.11	0.42
	2	0.38	0.46	0.44	0.55
	3	0.18	0.35	0.23	0.46
	4	0.37	0.47	0.44	0.55
	5	0.18	0.34	0.23	0.48
4	1	0.14	0.55	0.15	0.59
	2	0.51	0.66	0.53	0.67
	3	0.21	0.51	0.23	0.55
	4	0.53	0.66	0.54	0.68
	5	0.23	0.49	0.24	0.55

Table 3: Comparison of maximum delays between the twisted-bundle and normal structures.

Length,freq	Maximum delay (*ns*) Twisted Structure: twisted	Twisted Structure: normal	Normal Structure
1*mm*,1*GHz*	0.040	0.041	0.041
1*mm*,2*GHz*	0.033	0.033	0.034
2*mm*,1*GHz*	0.069	0.073	0.072
2*mm*,2*GHz*	0.061	0.067	0.065
4*mm*,1*GHz*	0.140	0.146	0.145
4*mm*,2*GHz*	0.129	0.138	0.137

switching signals switch at the same time. Table 2 shows the noise levels measured at the far end of the victim signal 8. From the simulation results, we observe that the twisted-bundle structure can effectively reduce the coupling noise. For 1*mm* wire, we achieve 4% to 72% noise reduction; for 2*mm* wire, 18% to 76%; and for 4*mm* wire, 20% to 75%. Similar results are obtained when we use input patterns obtained by substituting '1' for '0' and '0' for '1' in the five input patterns listed in Table 1.

The impact of the twisted-bundle structure on signal delay is also investigated. The input patterns are similar to those in Table 1 except that signal 8 is also switching (both high and low) instead of being quiet. Table 3 summarizes the maximum delays found for the twisted-bundle and normal structures. The second and third columns in Table 3 list the maximum delays of nets in the twisted groups and normal groups of the twisted-bundle structure, respectively; the fourth column lists the maximum delays of nets in the normal structure. Although every wire in a twisted group has a longer wire length, a higher resistance, and a higher capacitance than wires in a normal group, the simulation results show that wire twisting has minimal impact on the maximum delays. The maximum delays for twisted wires and normal wires in the twisted-bundle structure do not differ by more than 10%. The differences between the maximum delays of the twisted structure and normal structure are even smaller.

6. CONCLUSION

In this paper, we present the *twisted-bundle* layout structure. Inductance extraction with FastHenry shows the effectiveness of this structure in minimizing mutual inductance. SPICE simulation results also show that it can considerably reduce the coupling noise.

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